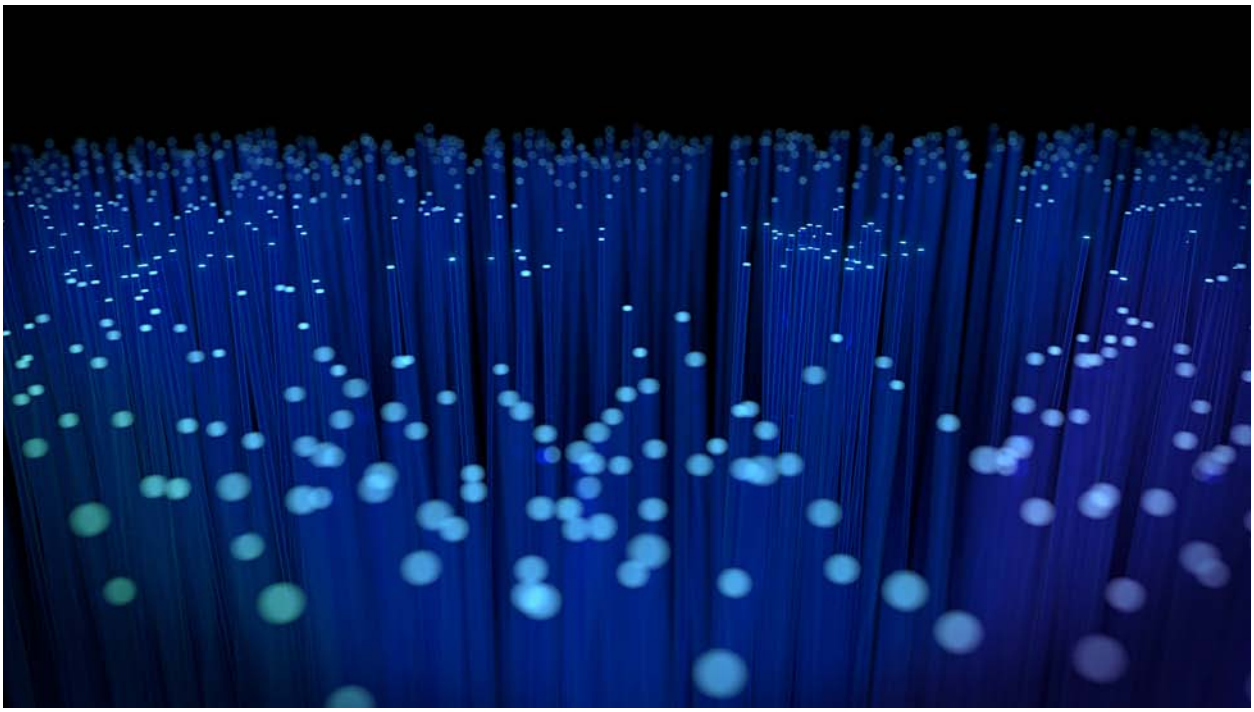
PSMC

Photonic Systems Manufacturing Consortium

2015 ROADMAP

DECEMBER 2015



A collaborative effort between the International Electronics Manufacturing Initiative (iNEMI) and the MIT Microphotonics Center.

Funded by the NIST Advanced Manufacturing Technology Consortia (AMTech) Program

PSMC TECHNOLOGY ROADMAPS

December 2015

FOREWORD

As we near completion of the first phase of our Photonic Systems Manufacturing Consortium's (PSMC) Five Year Sustainability Plan, we are releasing the first edition of the *2015 PSMC Integrated Photonic System Technology Roadmaps.* This first PSMC Roadmap builds on the processes used and lessons learned from previous roadmap developments by the two PSMC Partners: The International Electronics Manufacturing Initiative and the MIT Microphotonics Center.

In spite of the fact that most companies and individuals are "oversubscribed" in their day jobs, approximately 400 professionals from more than 11 countries, representing more than 160 organizations, came together to create this product. Through sharing, analyzing, debating and reviewing, this diverse team contributed to these first roadmaps.

PSMC Sustainability Mission Statement: The PSMC will become a vital, industry-sustained infrastructure element within the next five years. The PSMC value proposition is based on three pillars: Roadmap, "Big M" Technology Evaluation, and Supply Chain Integration. The pace of value creation is dependent on the emergence of cost effective, platform-based, high volume photonics manufacturing. Significant adoption of integrated photonics manufacturing is required during the next five years for PSMC to meet it sustainability goals.

In July 2015 Vice President Biden announced that AIM Photonics was awarded the Integrated Photonics Institute for Manufacturing Innovation (IP-IMI). PSMC had committed in our Sustainability Plan and April 2015 Semi-Annual/Technical Progress Report to support the IP-IMI. The PSMC Principal Investigators had communicated with the three contenders for the IP-IMI DOD Award. The PSMC Principal Investigators committed to play a major role in the Administration's Institutes for Manufacturing Innovation and subsequent entities under AMP (Advanced Manufacturing Partnership). 2.0 PSMC will cooperate and support all AMP entities in the development of a strong US integrated photonics manufacturing base. Professor Lionel Kimerling, PSMC Co-Principal Investigator has been appointed Executive of the AIM Photonics Academy, and Dr. Robert Pfahl PSMC Co-Principal Investigator, has been appointed Leader of the AMP Photonics Integrated Photonics Technology Roadmap.

The remaining task in Phase 1 of our Sustainability Plan is to develop a "PSMC Technical Plan." We will begin this process December 7, 2015 at the PSMC Workshop at MIT where participants will develop prioritized lists of gaps for each Technology Working Group. In the coming months these lists will be the foundation for AIM Photonics to develop a technical plan to help guide the selection of future R&D projects.

For our next roadmap we plan to add additional Technology Working Groups (TWGs) and Product Emulator Groups (PEGs) to address needs identified by AIM Photonics. We will begin this process with the formation of a Modeling, Simulation, and Design Tools TWG and a Sensors TWG in December.

We welcome your thoughts and comments as you use this important reference document in your planning processes.

Dr. Robert C. Pfahl, Jr.

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Senior Consultant, iNEMI

Dr. Lionel C. Kimerling

Principal Investigator, PSMC
Thomas Lord Professor of Materials Science, MIT

ACKNOWLEDGMENTS

NIST AMTech

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We extend special acknowledgment to those contributors who drafted, edited and summarized the materials in this document:

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- Richard Otte, Promex Industries, Integration TWG Chair
- John L. MacWilliams, Bishop Associates,
  - Chair, PSMC Interconnect (Connectors & Substrates) TWG
- Richard Grzybowski, MACOM,
  - Chair, PSMC Internet of Things (IoT) Product Emulator Group (PEG)
- Randolph E. Kirchain, MIT, Emulator Cost Modelling Co-Chair
- Elsa A. Olivetti, MIT, Emulator Cost Modelling Co-Chair

Technology Working Groups and Product Emulator Group Members.

The Technology Working Groups (TWGs) and Product Emulator Groups (PEGs) include a large number of industry, academic and government professionals. Members of each TWG are listed at the end of each Technology Roadmap. A complete list of roadmap participants can be found in *Appendix C*. More than 400 professionals from more than 11 countries, representing more than 166 organizations took the time to participate actively in the PSMC Roadmapping process either through the TWGs and PEGs or during three roadmapping workshops. Although we value the work of all participants and have made every effort to include them in these acknowledgments, probability dictates that a few organizations and/or individuals may have been left out. If that is the case, we apologize for any inadvertent oversight. Please note that the professional participants listed are respected as visionaries in their respective fields, and their views are not necessarily a reflection of the views of the entities where they work.

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INTRODUCTION

On May 9, 2014 the National Institute of Standards and Technology (NIST) announced 19 advanced manufacturing technology grants awarded in the Advanced Manufacturing Technology Consortia (AMTech) Program. The Photonic Systems Manufacturing Consortium (PSMC), a consortium formed between the International Electronics Manufacturing Initiative (iNEMI) and the MIT MicroPhotonics Center - had anticipated the awarding of this grant and conducted its first Roadmapping Workshop in April 2014 to begin implementing the first of three phases of their proposal.

- Phase 1 Planning
- Phase 2 Execution of Plan
- Phase 3 Self-Sustaining Institute

PSMC received a grant of $540,000 to execute the first phase of the program. During Phase 1 the PSMC is developing a strategic Roadmap and Technical Plan that i) identifies critical technical requirements for next-generation system integration and packaging, ii) details potential solutions to meet those requirements economically, and iii) identifies the technology supply chain limitations for commercial deployment of the required component performance in the 2015-2035 time frame. The Roadmap is responsible for i) promoting Design for Manufacturing (DfM) philosophy and ii) raising the issue of packaging science and engineering to significance for academic research and for allocation of industry and government resources. Three dedicated Workshops, two of which have been completed, are developing and cementing the Phase 2 goals.

The PSMC program addresses i) the unprecedented growth of data centers, ii) the increasing volume of internet traffic, and iii) the introduction of short reach optical interconnection in distributed architectures for communication, computing and sensing. The continued scaling of this massive growth and accompanying architecture changes requires the creation of a platform for the high-volume, low-cost manufacturing of integrated photonics. The nation that establishes the system design-for-function capability to address these needs, and the high volume, low cost infrastructure to manufacture high performance, energy efficient hardware will dominate the industry.

PHASE 1: PLANNING

The PSMC strategy is centered on building a common manufacturing ecosystem that supports the Technology Supply Chain. The key outcomes of the Phase 1 planning stage are i) building mutual trust and cooperation among the supply chain stakeholders to establish a common vision for high volume photonic system manufacturing and for the technology gaps that need to be closed and ii) developing a cohesive roadmap for integrated photonic system design.

The PSMC Roadmap projects that a 1000 X increase in photonic system performance must be achieved at constant cost during the next decade. The advance of functional performance will require coordination of architecture, hardware, software and new application developments. Today's leading commercial firms may not be capable of surviving the reduction in margins as production volume is ramped higher. The PSMC is positioning its constituency to be the

complete Technology Supply Chain from materials-and-tools to end-users. The key to sustaining the Consortium Value Proposition is commercial application of the benefits of i) identifying roadblocks, ii) developing new technology and iii) practicing that new technology to build a common manufacturing learning curve. The PSMC strategic plan provides for ongoing Consortium-based development for the next 30 years.

The PSMC sustainability model for research, development, and manufacturing (RD&M) presumes development of a strong U.S.-centric supply chain that will draw industrial funding to the domestic research community to enable manufacturing growth. The PSMC Roadmap will continue, with the support of iNEMI and MIT Microphotonics Center, the specification of components, materials and technology needs at the system level.

The overarching goal of Phase 1: Planning is to create the processes and infrastructure necessary to conduct focused research and development during Phase 2. During Phase 1 we have integrated the roadmapping efforts of iNEMI and of the MIT Microphotonics Center to address the systems needs and the manufacturing needs of integrated photonics. We have organized the goals of the Phase 1: Planning into three "stages:"

- Stage 1: Initial Roadmap Development
- Stage 2: "Emulator" Development to Quantify needs
- Stage 3: Creation of the R&D "Technical Plan"

The Photonic System Manufacturing Consortium (PSMC) has facilitated a strong working relationship among the stakeholders to address both the research needs and the required manufacturing infrastructure for integrated photonics. To date more than 400 stakeholders from more than 160 organizations have participated in PSMC activities. This structure will serve the nation well in the Phase 2 execution phase of cooperative research and development to address the critical challenges for integrated photonics that are identified in the Roadmap.

The remaining task in Phase 1 of our Sustainability Plan is to develop a "PSMC Technical Plan." We will begin this process December 7, 2015 at the PSMC Workshop at MIT where participants will develop prioritized lists of gaps for each Technology Working Group. In the coming months these lists will be the foundation for AIM Photonics to develop a technical plan to help guide the selection of future R&D projects.

PHASE 2- EXECUTION

In July 2015 Vice President Biden announced that AIM Photonics was awarded the IP-IMI (Integrated Photonics Institute for Manufacturing Innovation). PSMC had committed in both our Sustainability Plan and our April 2015 Semi-Annual/Technical Progress Report that we would support the IP-IMI. The PSMC Principal Investigators had communicated with the three contenders for the IP-IMI DOD Award. The PSMC Principal Investigators committed to play a major role in the Administration's Institutes for Manufacturing Innovation and subsequent entities under AMP (Advanced Manufacturing Partnership). 2.0 PSMC will cooperate and support all AMP entities in the development of a strong US integrated photonics manufacturing base. Professor Lionel Kimerling, PSMC Co-Principal Investigator has been appointed Executive of the AIM Photonics Academy, and Dr. Robert Pfahl PSMC Co-Principal

Investigator has been appointed Leader of the AMP Photonics Integrated Photonics Technology Roadmap.

In the Phase 2 of PSMC activities we will offer our experience in establishing an organization dedicated to manufacturing innovation; we will provide data and analyses based on our industry-wide strategic Technical Working Groups. The PSMC Technology Roadmap and supply chain coordination are critical elements for the AIM Photonics missions of manufacturing technology implementation and job creation. Definition of technology roadblocks and potential solutions will help structure AIM Photonics requirements; and technology timelines and cost analyses will help forecast the pace and content of the Education and Work Force Development in support of job creation. The PSMC technology targets, production and market data, and gap analyses will give continuous guidance to the IP-IMI strategic objectives.

PSMC WORKING GROUPS

PSMC Technology Working Groups (TWGs)

During Phase 1 we have integrated the roadmapping efforts of iNEMI and the MIT Photonics Center to address both the systems needs and the manufacturing needs of integrated photonics. The four Photonic Systems Manufacturing Consortium (PSMC) Technology Working Groups (TWGs) have been established and are developing the roadmap. They are similar to existing iNEMI and Microphotonics Center TWGs, but they differ in scope. PSMC has been added to all TWG titles to mark this distinction in scope. The PSMC TWGs include many members from existing iNEMI-MIT groups, but their charters are more focused.

Since August 2014 the TWG leaders have been recruiting additional members and working with their TWGs. The four PSMC Technology Working Groups (TWGs) and their leaders are:

- PSMC Monolithic Integration TWG: Lionel Kimerling, MIT
  - Chips: silicon photonics, InP
  - Tradeoffs for cost, bandwidth density, power efficiency, and functional latency
- PSMC Packaging TWG: Bill Bottoms, Third Millennium Test Solutions:
  - Cost, materials, heat, footprint, port count, bandwidth, integration, functionality
- PSMC Interconnect (Connector & Substrate) TWG:
  John MacWilliams, Bishop &Associates
  - Connectors includes: all separable interfaces within the system scope
  - PSMC Assembly and Test TWG: Dick Otte, Promex Industries
  - Design for Manufacturing
  - Assembly and Test
  - Supply Chain Trade Offs

PSMC Monolithic Integration TWG

This PSMC TWG addresses chip-level integration on the Si and InP platforms; design for manufacturing; and tradeoffs for cost, bandwidth density, power efficiency, and functional

latency. The long term view will include identifying functional optical components such as optical switching. The chair of this TWG is Lionel Kimerling: lckim@MIT.EDU

PSMC Packaging of Electronic Photonic Systems TWG

This PSMC TWG focuses on the Packaging Technology and cost objectives needed to meet market requirements for low cost high volume photonic components and sub-systems for integration into the global network. Cost and performance objectives for system level, board level, package level and, where it is practical, chip level integration of photonics are the initial focus. Members will develop the needs for cost, materials, thermal, footprint, port count, and bandwidth. The chair of this PSMC TWG is: Bill Bottoms: bill_bottoms@3mts.com

PSMC Interconnection (Circuit boards, Backplanes and Connectors) TWG

This PSMC TWG covers the intra-system connector and circuit board technology that will be needed for integrated photonic systems. Connectors include all separable interfaces within the system scope. Substrates include all circuit board and backplane components. The chair of this PSMC TWG is John MacWilliams: jmacwilliams@bishopinc.com

PSMC Assembly and Test TWG

This PSMC TWG addresses the development of manufacturing processes, materials and equipment to produce integrated photonic systems with ever decreasing cost and increasing volume. The PSMC TWG covers the needs for cost, integration, assembly, test, functionality, and tools. The chair of this PSMC TWG is Dick Otte: otte@promex-ind.com

PSMC Product Emulator Groups (PEGs) and Cost Modelling

In addition to the TWGs the PSMC working groups also includes Product Emulator Groups (PEGs) and an emulator group developing a cost model. The two Product Emulators have been defined utilizing input from the MIT Microphotonics Open Architecture System Optimization (OASO), the Leadership Committee, and the Executive Advisory Board (EAB). The emulators define the application needs and system performance targets, based upon an understanding of the consequences of parallelism, virtualization, and software defined networks.

PSMC Data Center PEG

Data centers are a critical node of network architecture that is driving higher bandwidth from the core network to ever shorter distances. As single channel data rates exceed 10Gb/s, copper transmission lines introduce excessive loss, necessitating a transition to photonic interconnects. The pervasive use of photonic interconnects at short distances means that photonic transport becomes a higher fraction of system data movement, requiring system design, architecture, software and hardware to be reconsidered. The Grand Challenges for information hardware are i) photonic integration for bandwidth density and ii) high volume manufacturing to meet the system demand. The chair of this activity is Bob Pfahl: bob.pfahl@inemi.org

PSMC Internet of Things (IoT) PEG

Chip-scale integrated photonic sensing systems are emerging as diagnostic sensors for medical, environmental and security applications; structural health monitoring; military sensing; and wireless sensor networks – the entire Internet of Things (IoT) space. The field is advancing rapidly, with fabrication technologies that leverage standard microfabrication infrastructure and enable the co-integration of sensors, photonics, electronics, and microfluidic sample preparation systems. The chair of this activity is Rich Grzybowski: Rich.Grzybowski@macom.com.

PSMC Cost Model Development

PSMC is developing technology-based models for the cost, energy, and environmental implications of various component and architecture alternatives for the two emulators under consideration. These process-based cost models (PBCM) will enable the modeling team to characterize how technologies will perform as photonics are integrated further into electronic systems. These tools also will serve to answer economic and energy use questions surrounding system architecture, enabling reliability and redundancy. Randolph Kirchain kirchain@mit.edu and Elsa Olivetti elsao@mit.edu are developing the PSMC cost emulator.

EXECUTIVE SUMMARY

SITUATIONANALYSIS

MARKET

The boundaries among computers, communications and entertainment products have blurred. Flat panel displays are the norm for virtually all applications, with touch screen technology becoming dominant in a number of product categories. Wireless products continue to proliferate and this is opening up new applications in a number of segments. We are seeing dramatic growth of mobile Internet applications, including the massive demands for mobile data, the growth of mobile video, and the dramatic increase of smart phones as the gateway to the web.

According to a June 2014 report from Cisco Systems, annual global IP traffic will surpass the zettabyte (1000 exabytes) threshold in 2016, and reach 1.1 zettabytes per year in 2016. Global IP traffic has increased more than five-fold in the past five years, and is expected to increase three-fold over the next five years. Overall, IP traffic is forecast to grow at a CAGR (Compound Annual Growth Rate) of 21% from 2013 to 2018.

End users desire more integrated, 'open-source' data center systems and the end users have emerged as a powerful factor in data center hardware selection. Consequently the center of power has shifted from OEMs to the large end users. The end users are establishing specifications for cost, energy, and bandwidth density. To reach their performance goals they are evaluating the impact of disaggregation, virtualization, direct memory access and microservers.

Today integrated optics technology is proprietary and not manufactured in high volume. Having multiple supply chain sources is difficult. Establishment of an enabling silicon photonics technology as envisioned in this roadmap is a necessary step to achieve low-cost, high-volume manufacturing in this rapidly expanding market.

The Internet of Things (IoT) ecosystem is hard to define, complex, and difficult to capture due to the vast possibilities and the rapidity with which it is expanding. The available technology is being developed faster than new market opportunities can be identified. Key technologies for this market are improved low-power, high-speed communications and new sensors. These are technologies that integrated photonics systems are well positioned to address. The success of IoT depends strongly on standardization, that provides interoperability, compatibility, reliability, higher manufacturing volumes, and effective operations on a global scale.

TECHNOLOGY

Cisco Systems projects that, globally in 2018, IP video traffic will be 79% of all consumer internet traffic, a five-year increase of 13%. This percentage does not include video exchanged through peer-to-peer (P2P) file sharing. The sum of all forms of video (TV, video on demand, Internet, and P2P) will be in the range of 80-90% of global consumer traffic by 2018. The telecommunications system and everything down to semiconductor chips must grow proportionally in both capacity and performance to support that traffic increase. In addition, new mobile applications require large amounts of computing power

resulting in warehouse computers that consume 50+ megawatts. These changes drive optical technologies. As these data rates increase, optical methods are replacing copper/electronic methods at ever shorter distances. The current transition point is at data rates of 10 Gb/s and distances of 1 to

10 meters. When data rates or distances greater than those are needed, optical methods are attractive because they often reduce both power consumption and physical size up to 75%.

High-density 3D packaging of complete functional blocks has become the major technology challenge. By the end of 2019, CMOS process capabilities are forecast to be augmented by multiple new devices to implement functions beyond those of CMOS devices. However, since all of these new devices are unlikely to be compatible with CMOS processes, heterogeneous integration — either at the chip level or at the package level — will be needed to combine these new capabilities around a CMOS core. It is anticipated that this integration will be the most cost effective solution for silicon photonics.

- System-in-package (SiP) applications for portable products have become the technology driver for small components, packaging, assembly processes and high-density substrates.
- The demand for MEMS devices that provide higher performance, lower cost, new functions and integration of multiple sensor functions has led to the development of complex devices such as tri-axis accelerometers with gyroscopes and magnetometers, enabled new sensor device technologies, and advanced signal processing and communications interfaces.
- The interactions of light with matter are the basis for a variety of sensors that incorporate electronics for data processing and communications, either RF, electrical and optical.
- According to Yole Development, the first memories integrating 3D through silicon via (TSV) technology are in volume production, taking full benefit of MEMS processes.

HIGHLIGHTED NEEDS

- During the 15 year life of this roadmap we must change the global network, the components in it and most of the elements attached to it, in order to meet the market needs of:
- 10^4 improvement in power efficiency
- 10^4 improvement in cost per function
- 10^6 improvement in the number of network ports

All of these improvements are needed at no increase in total cost!

The potential sources of improvement are these:

1. Disaggregation to improve the utilization of microprocessors from 15% to close to 100%. 5X
2. Microservers to replace blade servers. 10X
3. Direct memory access vs going through the internet protocols in data centers. 10X

4. Broad implementation of circuit switching and switching in the optical domain. 10X
5. Further improvement in devices i.e. More Moore meaning CMOS at 10 nm nodes. 5X.

Optical methods that reduce power and increase data density will be widely used to implement these improvements.

More importantly, achieving this challenging task will require that the mechanisms for cooperation between industries and among researchers who are working in all advanced technologies must be strengthened. Cooperation among OEMs, ODMs, EMS providers and component suppliers is needed to focus on the right technology and to find a way to deploy it in a timely manner.

As noted in the introduction to this roadmap, the key activities of PSMC since May 2014 have been i) building mutual trust and cooperation among the supply chain stakeholders to establish a common vision for high volume photonic system manufacturing and for the technology gaps that need to be closed and., ii) developing a cohesive roadmap for integrated photonic system design.

The need for disruptive technologies to meet this challenge offer opportunity for innovation. In order to ensure success, the supply chain must be willing to invest with a long-term perspective in mind. The 2015 Roadmap has identified significant needs in a number of areas as highlighted in the following areas:

STANDARDS DEVELOPMENT

The need for standards development has been identified in a number of areas of the roadmap. Many roadmap participants believe that the lack of timely standards is slowing significantly the implementation of technology and growth of markets. Several consortia such as the Consortium for On-Board Optics (COBO) are working to create industry standards that allow:

- Interoperability
- Interchangeability
- Broader market potential

With the need for standards acknowledged, note that standards generally emerge as the industry finds they offer value and adopts them. Standards are generally not imposed from some higher level.

DESIGN TECHNOLOGIES

Design and simulation tools — or their lack of capabilities — can delay the rapid introduction of new materials and technologies. Particular areas where capabilities need to improve include:

- Modeling, Simulation, and Design tools for Integrated Photonic Systems;
- Design software able to utilize Hooke's General Law over temperature;
- Reliability, mechanical analysis and simulations;
  - Interfacial delamination,
  - Moisture modeling,
  - Material characterization, and

  - Process modeling.
- Prediction of lifetime based on physics of failure;
- Thermal and thermo-fluid simulations;
  - Passive thermal management,
  - Efficient and accurate thermal radiation, and
  - Increased need for system level simulations.

TRAINING OF DESIGNERS

Low cost, high-performance optical products start with good design. To effectively use this enabling technology requires that designers understand the technology and the manufacturing capabilities and limitations of the technology. Important factors that the designers need to understand include:

- Training of designers in Design for Manufacturing, Test and Cost;
- Minimizing the number of parts;
- Choosing parts that are adequate but not overly specified;
- Minimizing the number of assembly steps;
- Understanding details of parts and working with manufacturers to ensure that parts will have;
  - The necessary dimensional consistency,
  - Suitable location reference points,
  - Surfaces to which suitable joints can be made, and
  - Shipping package containers that interface with manufacturing assembly equipment;
- Evaluating the extremes of part specifications and dimensional tolerances to ensure robust design;
- Maximizing the tolerances required as best as possible; and
- Ensuring that dimensional requirements can be achieved.

MANUFACTURING TECHNOLOGIES

With research and development (R&D) responsibility shifting from OEMs to the ODMs and EMS companies, government, academia and industry consortia need to formulate new ways to adopt and develop emerging technologies into the manufacturing process. These new approaches will have to be consistent with viable business and funding required to create new industrial infrastructures. Specific manufacturing development targets include:

- Integrated photonics for high-volume applications,
- Process development to accelerate miniaturization,
- Assembly processes that support 3D structures and low-temperature processing,
- Cost-effective product traceability solutions,
- Anti-counterfeiting solutions,
- Reliability methodologies for manufacturing 3D structures, and

- Inspection/test technologies to keep up with increasing density of component packages.

MATERIALS

To meet the increased performance requirements of silicon integrated photonics will require the development of new materials with a variety of different properties. Insuring the reliability of these materials over the life of the product will be one of the gating issues for market introduction.

COMPONENT TECHNOLOGY

A standard approach to package and board level interconnection is required to achieve low cost of key components such as:

- Printed wiring boards with embedded waveguides,
- Embedded waveguide-to-surface layer connectors,
- Surface mount interposers and sockets,
- Surface mount optical transceivers ≥ 100-400Gbps, and
- Direct Chip-Attach Optical Interconnect.

SECURITY AND INFORMATION MANAGEMENT

Trusted foundries for military applications and component traceability, security, and anti-counterfeiting protection for all applications are issues that must be addressed as new enabling technology is introduced.

PARADIGM SHIFTS

The predominant paradigm shift identified in this Roadmap is the impact of cloud-connected digital devices. The movement to the cloud has the potential to cause major disruptions across the electronics and photonics industries. In the next few years, the industry is likely to see major transitions in business models. We expect to see more of the following:

- Huge data centers operating more like utilities (selling data services),
- Local compute and storage growth may slow (as data moves to the cloud), and
- "Rent vs. buy" for software (monthly usage fee for cloud based solutions).

Other paradigm shifts identified in the 2015 PSMC Roadmap include:

- The need to continuously introduce complex multifunctional products to address converging markets favors the use of modular components or SiP (2D, 2.5D & 3D),
- The "Internet of Things" (IoT) is making sensors ubiquitous; however, there are concerns about network security as cyber-attacks become more pervasive, and
- The disruptive technology required to produce a 1,000 X improvement in data center performance at constant cost.

STRATEGIC CONCERNS

- **Copper vs. Fiber:** Copper-based circuitry has advanced well beyond earlier capabilities and will continue to advance toward 100 GB throughput for short ~1m distances. There are companies working diligently on optical fiber solutions, but the number of companies doing this in the connector and PCB industries $\leq$ 10. There are a lot more making cable assemblies. At the core of optical fiber is one major US Company, Corning Glass.
- **Industry Cooperation**: Getting cooperation from industry personnel is difficult because of perceived IP issues involving their customers.
- **Cost Targets**: Proposed cost targets in an established industry are viewed as unrealistic unless standards are developed to commoditize the components.

KEY RECOMMENDATIONS

ROADMAPPING

For our next roadmap we plan to add additional Technology Working Groups (TWGs) and Product Emulator Groups (PEGs) to address needs identified by AIM Photonics. We will begin this process with the formation of a Modeling, Simulation, and Design Tools TWG and a Sensors TWG in December.

DESIGN

The increasing End User and OEM focus on time-to-market and the complexity of emerging technology requires significant development and investment in design tool infrastructure. The following areas need increased research and development:

- Reliability, mechanical analysis and simulations;
  - Material characterization including optical properties,
  - Interfacial delamination and chip-package interaction (CPI),
  - Process modeling,
  - Environmental stress modeling,
    - Moisture
    - Temperature cycling
    - Shock
    - Etc.
  - Joint reliability modeling,
- Research and development of thermal and thermo-fluid simulations;
- Tools and methodology research and development in the manufacturing systems/supply chain management areas;
- Projected development and research for simulations in emerging areas (e.g., photonics, nano devices and materials);
- Co-design of optical, mechanical, thermal and electrical performance of the entire chip, package and associated heat removal structures; and

- New capability to close the gap between chip and substrate interconnect density.

MANUFACTURING TECHNOLOGY

Manufacturing Technology has four strategic needs:

1. Miniaturization of the product,
2. Simplified, next-generation assembly processes,
3. Increased accuracy for assembling optical components, and
4. Fewer components to assemble.

These strategic needs generate the following recommendations in manufacturing technology:

- New approaches to organic substrate manufacturing that provide dramatic increases in density, reduced process variability, electrical performance and significant cost reduction;
- Manufacturing processes at all packaging levels to deal with warpage and thin format products;
- 3D package stacking development with emphasis on;
  - Assembly,
  - Testing,
  - Cooling, and
  - Reliability
- There are compelling advantages of 3D TSV technology; however, commercialization is gated by the development of the industry infrastructure and the supply chain;
- Low-temperature assembly, and
- Self-aligning assembly and stress free joining technology for photonic components.

MATERIALS DEVELOPMENT

- A combination of materials and fabrication research is needed to support the development of monolithically integrated optics and electronics that take advantage of the electronics infrastructure.
- Low-cost, higher thermal conducting packaging materials, such as adhesives, thermal pastes and thermal spreaders.
- New interconnect technologies deploying nano-materials to support decreased pitch and increased interconnect frequencies.
- High-performance laminates that are competitively priced.
- Clearer specifications for new materials, which are supported by a broad base of customers, to increase market size and reduce the risk for materials R&D.
- Reliability testing methodologies for new materials.

INTRODUCTION TO CHAPTER HIGHLIGHTS

A list of key roadmap drivers was developed for each of two product sectors, known as PEGS. Key parameters for the Product Sectors will be tabulated in *Appendix A* after the Fall 2015 PSMC Workshop.

The Technical Working Groups (TWGs) use the projected technology needs from Product Emulators as input for the TWG Roadmaps. If the global electronics infrastructure can meet or exceed the key Product Sector drivers, through implementation of the strategies discussed in the 2015 TWG Roadmaps, then the industry can enable faster technology deployment and increased growth in global market for electronic products. The focus of PSMC's implementation activities is to identify gaps and issues that would prevent us from attaining these key parameters. PSMC will then support AIM Photonics in developing a five year technology plan which proposes projects to address prioritized gaps.

Because of the broad coverage of these roadmaps, many acronyms from diverse fields appear in the text. For reading convenience, an effort has been made to define an acronym the first time that it is used in a chapter.

PRODUCT EMULATOR GROUPS

DATA CENTER PRODUCT SECTOR

The Data Center Product Sector Emulator covers the technologies that enable high-performance computing systems, data centers, and communications systems. The data explosion generated by the growth in social networks and digital entertainment, cloud-computing, and IoT are radically driving the growth of data centers and the need for high bandwidth, low-latency communication.

These forces are transforming the data center structures to a higher level of integration of computing, storage and networking components. The data bandwidth demand is resulting in systems with ever faster interconnect speeds, even as processor speed is staying constant. The size of the data centers creates a challenge for power demand creating an increasing focus on power efficiency of the systems. The data centers have an increasing number of systems residing in an environment of higher temperature, humidity and corrosive elements to reduce the operation costs and manage the total cost of ownership of these systems. Achieving this rapid growth places greater demands on increasing the performance and decreasing the cost of next generation equipment. Because of the capital requirements for adding capacity, all segments are undergoing rapid consolidation and movement to external cloud services.

The industry analysis by IHS projects a factory OEM revenue growth of 4.4% CAGR over the next 10 years from a cumulative $162B today to $273B in 2025. The growth in the Data Center sector is particularly strong, growing from $7B today to $22B in 2025 driven by the rapid increase in data traffic. The rate of innovation in the Data Center sector is high, enabled in part by the open source concepts of hardware and software. The Enterprise Communications sector is still recovering from the economic meltdown of 2008-2009 and upgrades are slow. However metro networks are heavily utilized, with the proliferation of 4G and investments including 100G interconnect. The Service Provider Equipment is more closely tied to short term economic trends and forecast growth of 5.4% CAGR is driven by technology upgrades and convergence.

The assembly and packaging technology to support the data centers continues to advance. In particular the need for high-speed, low-latency data transfer is driving the need for integrated silicon photonic components. The enabling technologies include:

- **Heterogeneous packaging** (Through-Silicon Vias (TSV) for stacked chips and silicon interposers,
- System in Package (SiP) and Package on Package (PoP),
- **integrated silicon photonics systems**,
- lower loss interconnect (low-loss laminates in printed circuit boards and packages,
- More efficient power conversion (wide band-gap materials).

The Data Center Emulator focuses on enumerating the trends over the next decade that integrated electronics components and technology must meet for the Data Center Market. These trends particularly focus on:

- packaging technology and costs,
- PCB and connector technology and costs,
- Testing and assembly/joining technologies.

INTERNET OF THINGS PRODUCT SECTOR

International initiatives like The International Year of Light (IYL) 2015, National Photonics Initiative (NPI), Horizon 2020, the BRAIN, and IP-IMI can only help reinforce what our industry already knows: Photonics plays a significant role in our daily lives and will only become more prevalent as future applications emerge!

The impact of IoT on daily life is expected to be as great as the impact the internet has had in the last two decades. Thus, the IoT is recognized as “the next phase of internet”. Enabling technologies include sensors and actuators, Photonics, Wireless Sensor Network (WSN), Intelligent and Interactive Packaging (I2Pack), real-time embedded system, Micro Electro-Mechanical Systems (MEMS), mobile internet access, cloud computing, Radio Frequency ID (RFID), Machine-to-Machine (M2M) communication, human machine interaction (HMI), middleware, Service Oriented Architecture (SOA), Enterprise Information System (EIS), data mining, etc. The IoT has, thus, become a new paradigm of the evolution of information and communication technology (ICT).

The IoT is expected to continually change and evolve – rapidly! More devices are being added every day and the industry is still in its infancy. Many of the challenges facing the industry are yet unknown. Given this, flexibility is needed in all facets of development. Processors and microcontrollers that range from 16–1500 MHz to address the full spectrum of applications from a microcontroller (MCU) in a small, energy-harvested wireless sensor node to high-performance, multi-core processors for IoT infrastructure. A wide variety of wired, wireless and photonic connectivity technologies are needed to meet the various needs of the market. A wide selection of sensors, mixed-signal and power-management technologies are required to provide the user interface to the IoT and energy-friendly designs.

The new technologies that are becoming available must meet these challenges – complexity, connectivity, security, bandwidth, power, and environmental. Key, new processor packaging technologies are being developed with some fundamental changes in the rest of the electronics

industry and how it impacts the technology that can be leveraged. With the IoT, a new set of technology will evolve, *but often at a much different scale of size, bandwidth and latency than required by typical data centers.*

COST EMULATOR

The goal of the PSMC roadmapping effort is to identify the opportunities, obstacles and potential solutions to realizing broad adoption of photonics in a range of applications. In doing so, the industry will have the opportunity to coordinate resources and overcome those obstacles more efficiently. With a technology which is rapidly evolving, many potential solutions will be proposed to realize the future photonics vision. Each of those potential solutions will not only need to be vetted to ensure that they will provide adequate performance (e.g., speed and size), but also for their potential economic ramifications. It will be important to target industry resources on the portfolio of solutions which promise both the best technical and economic performance.

To address the latter part of this challenge, the PSMC roadmap is in the process of developing a generalized cost modeling tool that can be applied to bound the cost implications of proposed solutions. The goal of such a tool can be simply stated: to quantify the cost implications of proposed process flows. Such information should allow the roadmapping teams to focus their resources more rapidly – earlier in the technology development process. Currently, the PSMC cost modeling tool focuses on the costs of packaging and assembly. The goal is to eventually expand that scope to encompass all relevant production related costs. This chapter delves into the motivation for creating such a tool and then describes the current state of the PSMC tool primarily through a case example of optical transceivers.

We limit our analysis to only the packaging of the optical devices into a module. The costs of components are taken as inputs and are not calculated directly. Although we carry out sensitivities to understand the potential implication of various levels of component costs, the reader should view this analysis as incomplete. Although incomplete, this analysis serves to demonstrate the potential for details process-based cost analysis to critical photonics questions.

Preliminary results suggest that:

- Monolithic integration of the Datacom transceiver has the potential to significantly lower packaging cost for both high and low volume production;
- The key cost savings opportunity for integrating in the near term derives from avoiding the expense of assembling and packaging the interposer layer;
- Integration has significant cost advantages even if optical chip yields were to fall well below baseline modeled values.

TECHNOLOGY WORKING GROUPS

Technology Working Groups (TWGs) in the 2015 Roadmap are:

- Monolithic Integration
- Integrated Silicon Photonics Packaging
- Interconnection
- Assembly & Test.

MONOLITHIC INTEGRATION

The PSMC Roadmap is a dynamic process, evident by the evolution of industry-wide semiconductor roadmaps over many years. The ITRS has reflected the semiconductor industry migration path from *geometrical scaling* to *equivalent scaling*. *Geometrical scaling* (e.g., Moore's Law) has guided targets for the previous 35 years, and will continue in many aspects of chip manufacture. *Equivalent scaling* targets improving performance through innovative system-level design, process, and software solutions that will increasingly guide the semiconductor industry in the future. Function-driven design requires incorporation of intelligent elements in the form of microprocessors, memory, and programmable logic devices built in silicon-based CMOS technologies. The *downscaling* of minimum dimensions enables the integration of an increasing number of transistors on a single chip, as described by Moore's Law. However, many quantitative requirements, such as power consumption and communication bandwidth no longer scale with Moore's Law.

Integrated Silicon Photonics research, development and commercialization initiatives address new functionalities that do not necessarily scale according to "Moore's Law".

- SiPh packages containing Si detectors, GaAs and InP lasers in SiP or PoP multi-chip designs.
- Fully integrated ICs that may in the future contain CPU/ASIC and Si photonic transceivers.

The so-called More-than-Moore approach typically allows for these functionalities to migrate from board-level modular applications, such as discrete transceiver packages and board-level interconnects, into a package-level (SiP), chip-level (SoC), Stacked Chip SoC (SCS) or Package-on-Package (PoP) solutions. What will a fully integrated Si-Photonic subsystem look like; and what are its design objectives? Table 1 depicts a likely path for this technology transition: discrete devices, to hybrid package assemblies, to integrated die functionality, to integrated photonic system-on-chip. Table 2 shows the projected integrated silicon photonics component deployment timeline.

Table 1. Silicon Photonics Technology Deployment

2015-16	2017-20	2020-25	Beyond
Discrete Devices	Interposers	EO CPU/ASIC	Logic-Memory-IO Integrated SiPh SoC Photonic Systems
EO Transceivers	InP VCSEL	Si Lasers	
Interconnect Modules	EO SiP/PoP	Multi-Die SiP	
MM Connectors	Fly-Over Cables	EO/Waveguide PCB	Wafer-Panel Substrates
MM Cables	MM-SM Connectors	SM Connectors	IO Connectors
AOCs	MM-SM AOC	SM Cables	Future WG

Interconnects Packaging SiPh Integration

Table 2. Silicon Photonics Components and Applications

Technology	Status
2015-16	
GaAs Lasers	VCSEL arrays commercially deployed in datacom
InP Lasers	Edge emitter arrays commercially deployed in telecom
Ge-on-Si Lasers	Research demonstration by several labs
Ge-on-Si Detectors	Fully waveguide integrated, commercially deployed
Waveguides	Si, SiON, SiN commercially deployed
SiP/SoC Assembly Technology	Electronics, but not photonics
Si Photonic Integration	Commercially deployed in cable and board assemblies
2017-20 Projected	
Ge-on-Si Lasers	Early market entry
Ge-on-Si Detectors	Pervasive commercial deployment
Waveguides	Pervasive commercial deployment, single channel
SiP/SoC Assembly Technology	Early 2.5 D deployment
Si Photonic Integration	Pervasive commercial deployment: cables and boards
2020-25	
Waveguides	Pervasive commercial deployment: WDM
SiP/SoC Assembly Technology	Pervasive commercial deployment: cables and boards
Si Photonic Integration	Emerging chip-to-chip intra-package
Beyond	
SoC Assembly Technology	Embedded in distributed circuit/system architectures
Si Photonic Integration	Transceiver-less: embedded electronic-photonic synergy

PACKAGING OF ELECTRONIC PHOTONIC SYSTEMS

Packaging is a limiting factor in electronics today since it has not kept pace with Moore's Law in scaling. Today electronic packaging is more expensive than the package contents in many cases and it contributes substantially to increased power requirements and latency. The solution to these limiting factors is a work in process with innovations such as wafer level packaging (WLP), system in package (SiP) architecture, 3D integration and heterogeneous integration. The integration of photonics into these emerging electronic packaging solutions is a focus of this Chapter but continued innovation in other areas will be essential.

There will be many specific challenges in realizing the benefits of integrating photonics into the fabric of the global network and the components attached to it. The solutions, however, cannot come from just packaging photonic components. The co-packaging of electronics, photonics and plasmonics will be required to address these substantial new challenges to meet the expanding requirement for higher performance, higher reliability, increased security, lower latency and lower cost of the future.

There will be new device types, new materials, new package production processes and new equipment required to accomplish these objectives. Some of these required innovations we know today but many specifics that must be addressed over the next 15 years are not known. The objective of this roadmap chapter is to identify the challenges with sufficient lead time so they solutions can be identified and proven before they become roadblocks to the pace of progress for the industry.

The difficult challenges for the global data network over the next 15 years will be reducing the size, cost, power requirement and latency while delivering greater bandwidth and increasing reliability and security. The primary enabling factor will be the development of low cost, high performance photonic integrated circuits. These developments will address many of the manufacturing costs associated with the mechanical assembly of components on a printed circuit board and maintaining the mechanical stability required for photonic circuits. Packaging has been a limiting factor in meeting these requirements and it must be a major contributor in defining solutions for the future.

The essential functions that a package must be provided include:

1. Protection for the contents of the package from the use case environment
2. Delivery of power for operation of the package contents
3. Provide data paths meeting bandwidth and latency requirements of use case application(s)
4. Isolation of signals internally to avoid noise and cross talk
5. Thermal and stress management to meet requirements of the package contents
6. Do no harm such as adding to power requirements and latency due to the package

These essential functions must be provided with the smallest size and lowest cost possible. The focus of this Chapter is identification of the difficult challenges and the potential solutions for meeting these challenges well in advance so the challenges do not become “roadblocks” to continued progress. The primary integration technology for the potential solutions will be a complex, 3D System in Package (SiP) architecture.

In order to identify the difficult challenges we are using two application areas from the Product Emulator Groups (PEGs) that will drive critical future requirements to focus our work.

INTERCONNECTION (CONNECTORS, CABLE ASSEMBLIES, PRINTED CIRCUITS)

Silicon Photonics technology (SiPh) is defined as photonic (lightwave) circuitry that employs low cost Si as a device and circuit platform and employs heterogeneous micro-packaging of various photonic chips and devices including GaAs, InP, and preferably Si micro-laser technology to drive low cost/high volume Computer/Datacom/Networking/Video Streaming applications. The compelling requirement for these technologies will be increasing circuit speed and bandwidth. These requirements are surfacing in high performance computing, data communication networks and data centers. Terabit speed will be necessary by the 2020s. OEMs recognize this paradigm shift from Cu to photonic circuitry. OEMs such as Cisco Systems, IBM and Intel are working on these technologies at the chip and system level. Intel has announced its Omni Path Interconnect Architecture which will provide a migration path between Cu and Fiber $\geq$ 40Gbps.

The Interconnect TWG encompasses the following Technologies:

Existing and Fiber Optic Connectors (Focus on Single-Mode Fiber)

Future EO Sockets and/or Interposers (EO Conversion from Metallic IC Package)

Existing and Future FO Cables and Transceivers (AOCs, Board-Level Transceivers)

Printed Circuit Boards (Organic FR4 Derivatives with Embedded Waveguides or Fibers)

Crosscutting Technologies covered in Packaging TWG:

Interconnects within a SiPh SiP Package (Packaging TWG)

Substrates employed in SiPh Multi-Chip IC Packaging (Packaging TWG)

Direct Chip Attachment of SM FO Cables (SiPh Device TWG)

Technologies Employed within the Semiconductor and IC Packaging Industries (Above)

Probable Future Technology Needs in Interconnect TWG:

#1: Surface Mount Silicon Photonics for High Speed and Bandwidth (≥THz) Data Center, HPCC applications

#2: Silicon Photonics MM Fiber in Internet2, IoT, Industrial, Medical and DOD applications for noise-immunity, environmentally rugged high speed and bandwidth applications (≤GHz)

Probable Future Interconnect Product Designs (*and Challenges*):

SM Fiber Optic Cable, PCB, IO Connectors (*Field Termination; Cost Targets*)

InP/Si RX/TX: Board-Level Modules, Active Cables (*MM Designs in Production; SM Future*)

Board Level Embedded Waveguide Connectors (*No Existing; Technology/Assembly/Cost*)

EOPCB with embedded waveguide and interconnect technologies

Chip to substrate or interposer electrical IO bump (copper pillar ?) densities down to <10 micron pitch from the ~50 micron in use today.

ASSEMBLY & TEST

The overall cost, including especially the cost for assembly and test, of optical devices needs to be reduced substantially to make optical products cost effective in more applications. Many of the most important potential applications require single mode technology where assembly of parts requires tolerances and stability of the optical chains over the lifetime of the product in the operating environment of less than 1 micron. Achieving that level of mechanical consistency at low cost requires starting with the design, selecting materials and structures to minimize the effect of temperature and stress and other environmental phenomena, selecting materials, joining methods, and assembly processes that will yield that result.

Generally, materials with high modulus and low TCE are best and have been used extensively in optical devices. Unfortunately these materials tend to be expensive so much effort is devoted to utilizing lower cost materials and the lower cost processes. Detailed mechanical and optical properties of the materials used in optical products are often not available. Standardizing on those materials and making the properties available will enable designers to model optical products better and minimize the need to build and test hardware.

An obvious way to avoid assembly cost is to minimize the number of parts to be assembled. That is being addressed through the increased use of integration. Unfortunately, all of the functions needed in optical applications cannot be integrated yet so assembly, or heterogeneous integration as it is often called, is needed.

Assembly methods and equipment from the microelectronics industry are often the initial choices considered for optical products. Many of these processes are perfectly suitable for optical devices, especially the electronic and non-dimensionally critical functions. In addition, a sub set of the electronic methods are effective for the high stability design and assembly methods. The chapter emphasizes the character of joining methods and highlights those standard processes, materials and equipment that are suitable for that demanding requirement. Thermocompression bonding, welding and UV cured polymers are often good choices.

Processes to achieve the 0.1 micron tolerances required for true passive alignment of optical devices are not widely available. Many approaches are being investigated to fulfill that need and avoid expensive (because it is slow and requires expensive equipment) active alignment where the optical chain is activated and used to actually ensure alignment is adequate.

A common request is for "equipment able to align parts to <0.1 micron of accuracy." Equipment to achieve that level of accuracy is not yet readily available. What is available is equipment able to achieve 0.5 micron accuracy. That capability needs to be improved. To capitalize on the resulting equipment, other steps are needed; overall design, inclusion of fiducials and reference points, selection of stable joining methods and joining materials, etc. In addition, improved interfaces to equipment are needed. These interfaces must reduce programming, set-up and change over times to minimize the cost to build high mix low volume optical products.

Optical test is complicated by the need to provide not only optical sources and detectors but usually similar electronic functions as well. The 10 to 100 GHz speed of many optical devices requires expensive equipment. In addition, optical signals have many parameters that need to be both generated and measured; wavelength, power, modulation rate, modulation method, polarization, etc., often for many channels simultaneously. 12 channels are common today with roadmaps forecasting over 1024 channels in the future. Providing all those sources and detectors results in complex, expensive test sets.

PSMC INTERNET OF THINGS PRODUCT EMULATOR

Contents

PSMC INTERNET OF THINGS PRODUCT EMULATOR

EXECUTIVE SUMMARY

International initiatives like The International Year of Light (IYL) 2015, National Photonics Initiative (NPI), Horizon 2020, the BRAIN, and IP-IMI can only help reinforce what our industry already knows: Photonics plays a significant role in our daily lives and will only become more prevalent as future applications emerge!

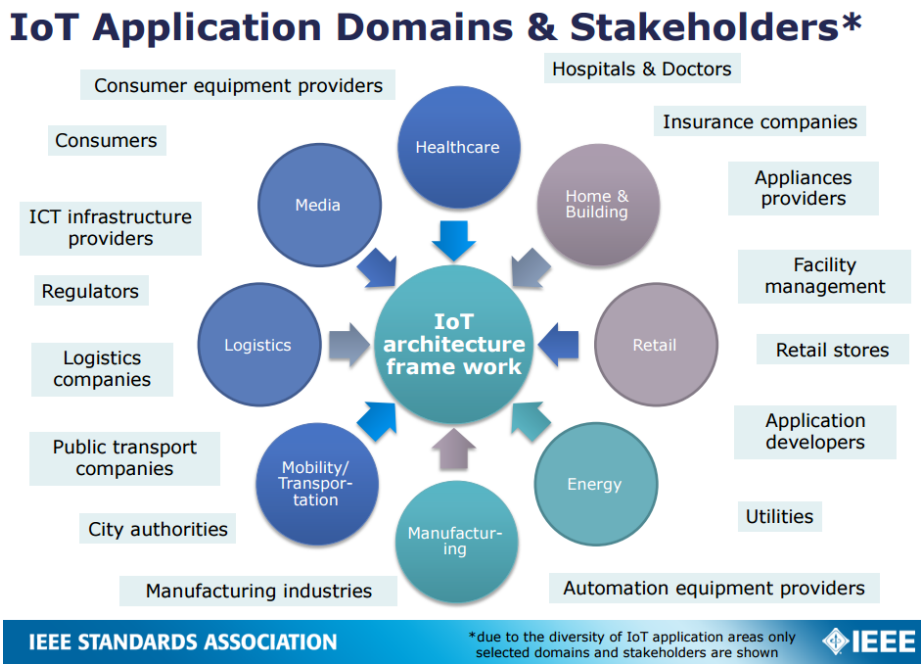
The impact of IoT on daily life is expected to be as great as the impact the internet has had in the last two decades. Thus, the IoT is recognized as "the next phase of internet". Enabling technologies include sensors and actuators, Photonics, Wireless Sensor Network (WSN), Intelligent and Interactive Packaging (I2Pack), real-time embedded system, Micro Electro-Mechanical Systems (MEMS), mobile internet access, cloud computing, Radio Frequency ID (RFID), Machine-to-Machine (M2M) communication, human machine interaction (HMI), middleware, Service Oriented Architecture (SOA), Enterprise Information System (EIS), data mining, etc. The IoT has, thus, become a new paradigm of the evolution of information and communication technology (ICT).

The IoT is expected to continually change and evolve – rapidly! More devices are being added every day and the industry is still in its infancy. Many of the challenges facing the industry are yet unknown. Unknown devices. Unknown applications. Unknown use cases. Given this, there needs to be flexibility in all facets of development. Processors and microcontrollers that range from 16–1500 MHz to address the full spectrum of applications from a microcontroller (MCU) in a small, energy-harvested wireless sensor node to high-performance, multi-core processors for IoT infrastructure. A wide variety of wired, wireless and photonic connectivity technologies are needed to meet the various needs of the market. A wide selection of sensors, mixed-signal and power-management technologies are required to provide the user interface to the IoT and energy-friendly designs.

The new technologies that are becoming available must meet these challenges– complexity, connectivity, security, bandwidth, power, and environmental. Key, new processor packaging technologies are being developed with some fundamental changes in the rest of the electronics industry and how it impacts the technology that can be leveraged. With the IoT, a new set of technology will evolve, but often at a much different scale of size, bandwidth and latency than required by typical data centers.

INTRODUCTION

The Internet of Things (IoT) is a key enabler for many emerging and future "smart" applications and technology shifts in various technology markets. They range from the Connected Consumer to Smart Home & Buildings, E-Health, Smart Grids, Next Generation Manufacturing and Smart Cities. It is therefore predicted to become one of the most significant drivers of growth in these markets.



Broadly speaking, the Internet of Things (IoT) is a system consisting of networks of sensors, actuators, and smart objects whose purpose is to interconnect "all" things, including every day and industrial objects, in such a way as to make them intelligent, programmable, and more capable of interacting with humans and each other. The IoT is loosely defined as connections between devices, cities and people. It is, in essence, the seamless flow between the: BAN (body area network): the ambient hearing aide, the smart t-shirts; LAN (local area network): the smart meter as a home interface; WAN (wide area network): the bike, car, train, bus, drone, etc. and; VWAN (very wide area network): the 'wise' city as e-gov services everywhere no longer tied to physical locations. The IoT is actually a collection of vertical markets and industries — and references the way they will be affected by connected devices and consumers. In all - the IoT ecosystem is hard to define, complex, and difficult to capture due to the vastness of possibility and the rapidity with which it is expanding. There is no common definition of IoT, but it is shaping the evolution of the Internet, creating numerous challenges and opportunities for engineering and science and the success of IoT depends strongly on standardization, which provides interoperability, compatibility, reliability, and effective operations on a global scale.

IoT is the subject of a great deal of hype and many bold predictions about where it will eventually take us. However, there is no question that IoT is changing the world. In addition to connecting people, anytime and everywhere, it is connecting IoT products to humans and other IoT products, and it is putting these products at the service of humanity. This transformation has already begun; it will only continue to accelerate. Note that there can be many IoTs. There is the global IoT (evolving from the global Internet) as well as local and private IoTs. The term "IoT" encompasses all of these.

The Internet of Things (IoT) IEEE Ecosystem Study Executive Summary January 2015, IoT products include devices, apps, and services (e.g., smart phones, tablets, intelligent networks, big-data analytics, and cloud storage). A key aspect of IoT is the intelligent connectivity of these products. (It is likely that there will be situations where devices will be more rigidly constrained to satisfy safety, legal, and regulatory obligations.)"

SITUATION ANALYSIS

THE IOT MARKET AND PHOTONICS

The IoT market is burgeoning but fragmented. Early players are active and currently creating products for which they see a market. These players include government and academia as well as business and industry. In order to get products to market, these players are implementing proprietary solutions, some of which may evolve into de facto standards. Currently, IoT is trending toward vertical applications. Verticals showing early growth are consumer-goods, eHealth, transportation, energy and industrial automation. IoT development and deployment is motivated by the desire to provide existing goods and services more efficiently (cheaper, faster, better) and by the desire to create new goods and services that will drive new revenue streams. Connecting things and allowing data to move will open new markets, just as the Internet did. New products and business models will disrupt traditional business models; some of these new products and models will be created by unintended consequences of technologies being deployed.

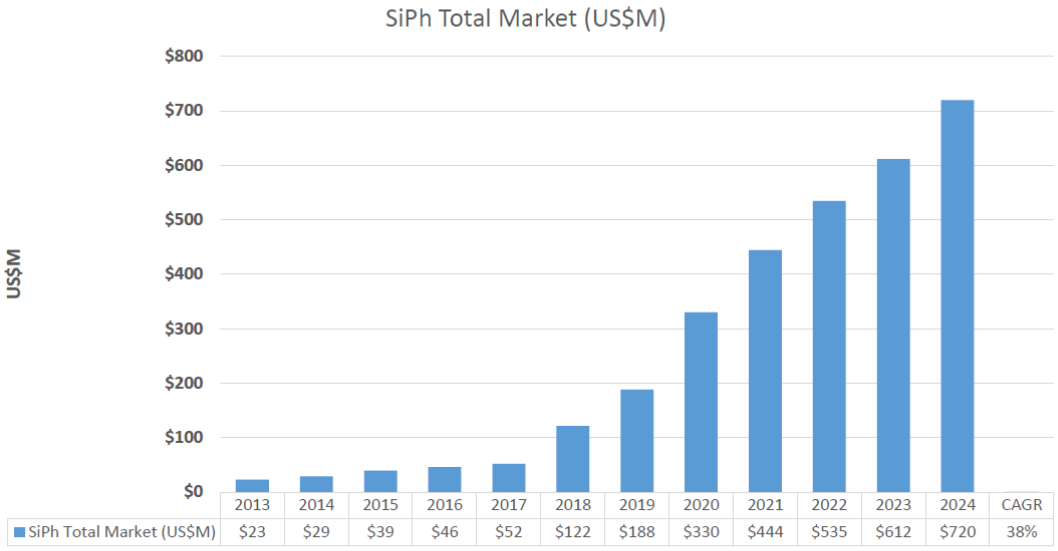
What might the value of the Internet of Things market be? Let's start at the top. You probably know that John Chambers, chairman and CEO of Cisco Systems, likes big numbers. In a keynote at the 2014 International CES in Las Vegas, he "pegged the value of the evolving IoT" to be $19 trillion! Chambers, in his keynote, gave many concrete examples: Cities saving money and increasing revenue by monitoring parking, lighting and water systems; connected homes with smart security and entertainment systems controlled by mobile apps; and eventually smart healthcare through an array of monitoring systems. "2014 will be a transformational, pivotal point for the Internet of Everything ... by 2017, it will be five to 10 times more impactful in one decade than the whole Internet has been," said Chambers. He described how IoT-based smart cities, for example, could see a direct return on investment through a smarter infrastructure. For quantitative backing, keynote guest speaker Antoni Vives, deputy mayor of Barcelona, Spain, said the city has saved $58 million a year using a smart water system, $37.5 million on smart lighting, and has increased parking revenue by one third through the use of smart parking meters.

According to a new market research report "Optical Networking and Communications Market by Technology (Wavelength Division Multiplexing (WDM), Synchronous Optical Networking (SONET)/ Synchronous Digital Hierarchy (SDH) and Fiber Channel), by verticals (Aerospace and Defense, Government, Manufactures, Submarine, Mining, Transportation, Oil and Gas, Healthcare, Telecom, Energy and Utilities) and by Geography - Global Trends & Forecasts to 2014 - 2020", published by MarketsandMarkets, the total value of optical networking and communications market is expected to generate revenue of $12.55 Billion in 2013 and is expected to reach $25.97 Billion by 2020, at an estimated CAGR of 10.5% from 2014-2020.

Similarly, MarketsandMarkets Internet of Things (IoT) Security Market by Technologies (Network, Cloud and Application Security, Identity Access Management, Analytics, UTM, IDS/IPS, Device Management, Encryption), Industry Verticals and Applications - Global Forecast to 2020 says that the integration of IoT has provided the control of different connected devices into a single smart device such as smartphones, PCs, and tablets and at the same time it has provided the opportunity to infiltrate the entire infrastructure by hacking the controlling device. Therefore, *IoT security* has become essential for the organizations, governments, utilities, and individuals for protection of data and infrastructure and is gaining traction in day to day deployment. IoT security market is driven due to rising security concerns in the critical infrastructures and strict government regulations and is expected to grow from USD 6.89 Billion in 2015 to USD 28.90 Billion by 2020.

Again, from MarketsandMarkets, the Silicon Photonics Market by Product (Photonic Wavelength, Optical Modulators, Optical Interconnects, WDMF, LED, and Others), Application (Telecommunication, Data Communication, and Others) and by Geography - Global Trends and Forecasts to 2014 – 2020 suggests that the silicon photonics is an emerging technology, which focuses on the ultimate goal of providing the microelectronics world with the ultra-large-scale integration of components at a low cost and without any significant changes in their performance. This can be achieved by producing the all-silicon based components and products. Hence, silicon photonics has become an interesting preposition across the globe as it focuses on high speed transmission, low cost, and high integration of various products together such as optical waveguides, modulators, and photo-detectors. The silicon photonics market is expected to grow to $497.53 million by 2020, growing at a CAGR of 27.74% from 2014 to 2020. This is rough order in line with Yole's prediction that the silicon photonics devices market will grow from less than $25 million in 2013 to more than $700 million in 2024 with a 38% CAGR.

Si photonics 2013-2014 market forecast in US$M



	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	CAGR
SiPh Total Market (US$M)	$23	$29	$39	$46	$52	$122	$188	$330	$444	$535	$612	$720	38%

Silicon photonics devices market will grow from less than US$25M in 2013 to more than US$700M in 2024 with a 38% CAGR.

YOLE Développement

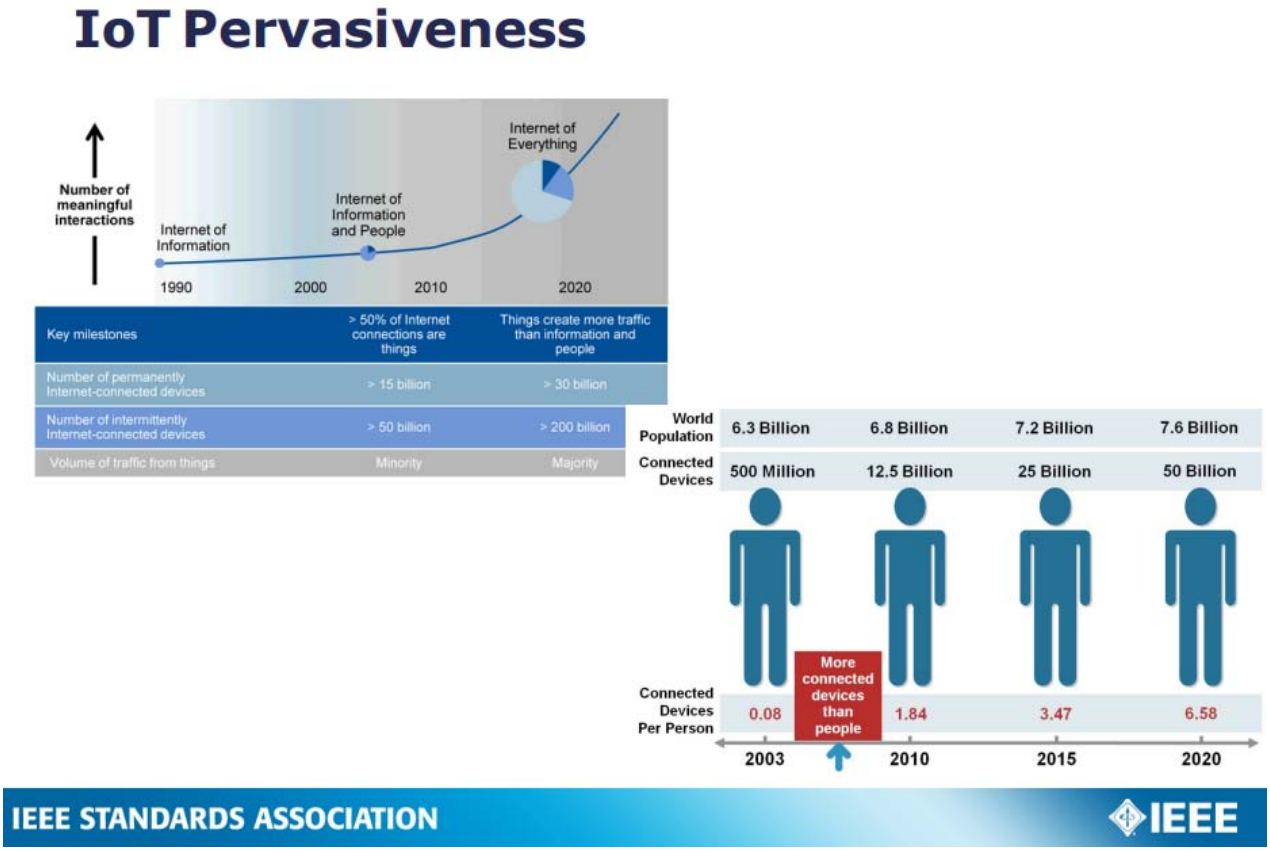
Technological advances are fueling the growth of IoT. Improved communications and network technologies, new sensors of various kinds, improved—cheaper, denser, more reliable and power efficient—storage both in the cloud and locally are converging to enable new types of products that were not possible a few years ago.

The potential impact of silicon photonics on the optical communications market has captivated the imagination of the industry in the last 3 years. Early success of several optical component vendors in the demonstration of capabilities of this technology and shipping first products led to several mergers and high value acquisitions. How much of an impact can this technology make on the market? Silicon photonics is garnering more value due to its various features and wide range of applications. It offers various advantages, such as high speed data transfer, data integration, and small factor form; moreover, since it is an emerging technology, it has managed to attract new industrial users. The telecommunication application held the highest market share in 2013, but the medical application is estimated to experience a better growth in the near future.

Silicon photonics is implemented by various companies in their product portfolios due to its advanced features, such as the high speed data transfer and integration of large data into a small device. Various products such as optical waveguides, modulators, and photo-detectors can be integrated within a single device, providing a smaller form factor with the help of silicon photonics. The Wavelength Division Multiplexer Filters (WDMF) and Silicon Optical Modulators (SOM) products currently hold the highest share in the North American market.

Thus, this shows that the WDMF and SOM products in the silicon photonics market have a great potential to increase over a period of time.

The MarketsandMarkets silicon photonics report http://www.reportsnreports.com/Purchase.aspx?name=273791) says silicon photonics has great potential as it is an emerging technology. This global report gives a detailed view of the market across geographies, namely Americas, Europe, Asia-Pacific, and RoW. The North American region dominates the market in terms of the market size; however, the APAC region has been growing at the highest CAGR in this market. The growing demand to transfer data and government funding in silicon photonics are motivating the companies to launch silicon photonics products in the North American market. The competitive landscape of the market presents a very interesting picture. The market is witnessing new product launches and large scale collaborations, and agreements and partnerships across the value chain, with a number of tier-one players around the globe. The major players in this market include Intel Corporation (U.S.), Hamamatsu Photonics, K.K (Japan), Finisar Corporation (U.S.), IBM Corp. (U.S.), Luxtera, Inc. (California), ST Microelectronics (Switzerland), 3S Photonics (France), Oclaro Inc. (U.S.), Mellanox technologies (U.S.), and Infinera Inc. (U.S.).



IOT CONNECTIVITY

Silicon photonics is emerging as a commercially available technology, vying for market share in a number of application spaces. For shorter distance applications (within and between rack) which continue to make up the bulk of HPC and data center links, silicon photonics must compete with the incumbent copper and VCSEL based technologies purely on cost and perhaps power. Here the functional advantages of Si photonics are more limited, albeit important, providing longer single mode reach at cost advantage over more traditional components. This is an expanding market space as both data rates and run lengths increase in flatter high performance networks. However this application does not take full advantage of the integration capabilities that Si photonics has to offer. Incipient deployment of optical circuit switched networks based on millisecond scale MEMs switching is beginning to show promise as a component of higher performance networks. Optical circuit switching is an application where silicon photonics can provide unmatchable technology advantages, by integrating a large number of functions on a single PIC, providing nanosecond scale switching times with reasonably large radix and integrated gain. While this application is still many years off, it is not achievable without the integration capabilities of a silicon photonics integrated circuit.

The inexorable rise of big data and the plethora of unstructured data being generated by connected devices and sensors are fundamentally changing datacenter economics, prompting a growing number of enterprises to consider greater IT virtualization or colocation as they adopt a hybrid cloud approach. Recent market research confirms that datacenter spending continues to increase. But retrofits are giving way to a growing focus on colocation or cloud services as the cost of building new datacenters becomes harder to justify.

Those trends, again driven by big data the IoT, are also being propelled by practical considerations like reducing latency in the datacenter as enterprises push data to the edge of networks. Meanwhile, hybrid and all-flash drives and storage are also being implemented as a way to reduce latency, note market analysts and colocation service providers.

Anticipating the shift away from corporate datacenters, colocation providers have been acquiring additional capacity. “Pushing data closer to the edge—closer to the businesses using the data—will become more important,” VXCHNGE noted in a blog post. “Having a datacenter that is closer to the people analyzing the data will increase speeds and reduce latency.” Colocation providers like VXchnge are betting that more enterprises will look to virtualization or colocation rather than investing in costly new datacenters. They are also wagering that customers will conclude that the increasing number of applications, workloads and IT infrastructure running on top of open-source technologies can be run reliably and at lower cost in the cloud. “Big data and the IoT will drive many changes in hardware, software, datacenters and more in the future,” VXchnge asserted. “To improve performance, companies will rely more heavily on pushing data to the edge.”

A recent datacenter spending survey bears out at least some of the colocation service provider’s assertions. Market researcher 451 Research found in a quarterly survey released earlier this month that 62 percent of respondents said they plan to consolidate IT infrastructure to accommodate power and space availability. Forty-one percent said they were looking to utilize

cloud service providers, including infrastructure-, platform- and software-as-a-service vendors as well as hosted private clouds. Only 25 percent of companies surveyed by 451 Research said they planned to build a new datacenter this year.

Moreover, it reported that datacenter consolidation and "migration projects" would translate into more high-end, centralized datacenters. Hence, the market researcher said overall datacenter square footage owned by global enterprises remains flat. If predictions about big data becoming a core enterprise capability prove true, market economics will likely fuel the shift away from datacenters to growing adoption of hybrid cloud infrastructure, market analysts say.

WEARABLES AND HOME DEVICES ARE LIKELY TO PLAY A LEAD ROLE IN IOT GROWTH. Wearables and home devices are likely to lead growth in the IoT business during the rest of this decade, according to semiconductor companies and industry analysts at the Computex Taipei show (June 2015). In 2015, 72 million wearable devices worth $17 billion will ship, growing in dollar terms at a compound annual growth rate (CAGR) of 18 percent to 156 million units or $39 billion in 2019, according to Bryan Ma, a vice president with market research firm IDC.

But what device is likely to be the wearable of choice? "If I were a betting man, it would be watches," said James Bruce, director of mobile solutions for ARM, whose chip designs are in 90 percent of the world's smartphones," in a Computex presentation. "Wristbased products are definitely going to be one of the leading categories. We're at the start of that growth."

Overall, the worldwide IoT market will grow from $655.8 billion in 2014 to $1.7 trillion in 2020 for a CAGR of 16.9 percent, IDC said in a June 2 report. That growth forecast appears less optimistic than a prediction this month by market watcher Linley Gwennap for a CAGR of 45.5 percent in IoT unit shipments between now and 2020. Gwennap said 1.9 billion IoT devices will ship in 2020, up from about 200 million this year.

It will take time for wearables to become compelling, according to ARM. "It took years for smartphones to develop their various use cases," Bruce said. "We're now seeing the same thing with wearables. Three or four years down the line, you'll see lots of different people using wearables." For mobile payment or access to a home or a car, a watch with near field communication (NFC) makes sense because of the ease of use, Bruce said. For home IoT devices, use cases are developing rapidly in China, according to MediaTek, the world's third largest chip designer. "The home IoT market in China is growing faster than the rest of the world," said SR Tsai, general manager of MediaTek's Wireless Connectivity and Networking Business Unit, in an interview with EE Times. The home IoT market worldwide this year will reach 50 million units.

The home IoT market worldwide this year will reach 50 million unit shipments and 200 million units in the next three years, Tsai said. That forecast converts into a bullish CAGR of 59 percent for the 3 year period. In China, some companies have started adding WiFi controlled smart switches to air conditioners and other home appliances, according to Tsai. China's Xiaomi, the world's third largest smartphone maker, and other local handset makers are trying to deploy IoT as part of their business, Tsai said. Helping to stimulate demand, the Chinese government will

invest about $200 billion during the next three years in domestic broadband access for fiber to the home at a 10 gigabit per second rate, he added.

Of course, security issues may become a limiting factor in China's burgeoning home IoT business, according to Tsai. "Their security concerns are lower than in other areas," he said. "Smartphones are the personal gateway, but you still need a home gateway." According to research by security software vendor Trend Micro, about 30 percent of the routers in the marketplace have been hacked, Tsai said. MediaTek and Trend Micro have allied to provide security against attacks on home networks. "If your router transfers a lot of data outside, we can stop this kind of attack," according to Tsai. "Rather than securing the end device, as with laptops years ago, now it's better to secure at the gate in home routers." In a smart home, air conditioners, refrigerators and doors are links in the network that could potentially leak valuable personal data to outside hackers, Tsai says. "If they are breached, you are in big trouble."

SENSORS IN THE IOT

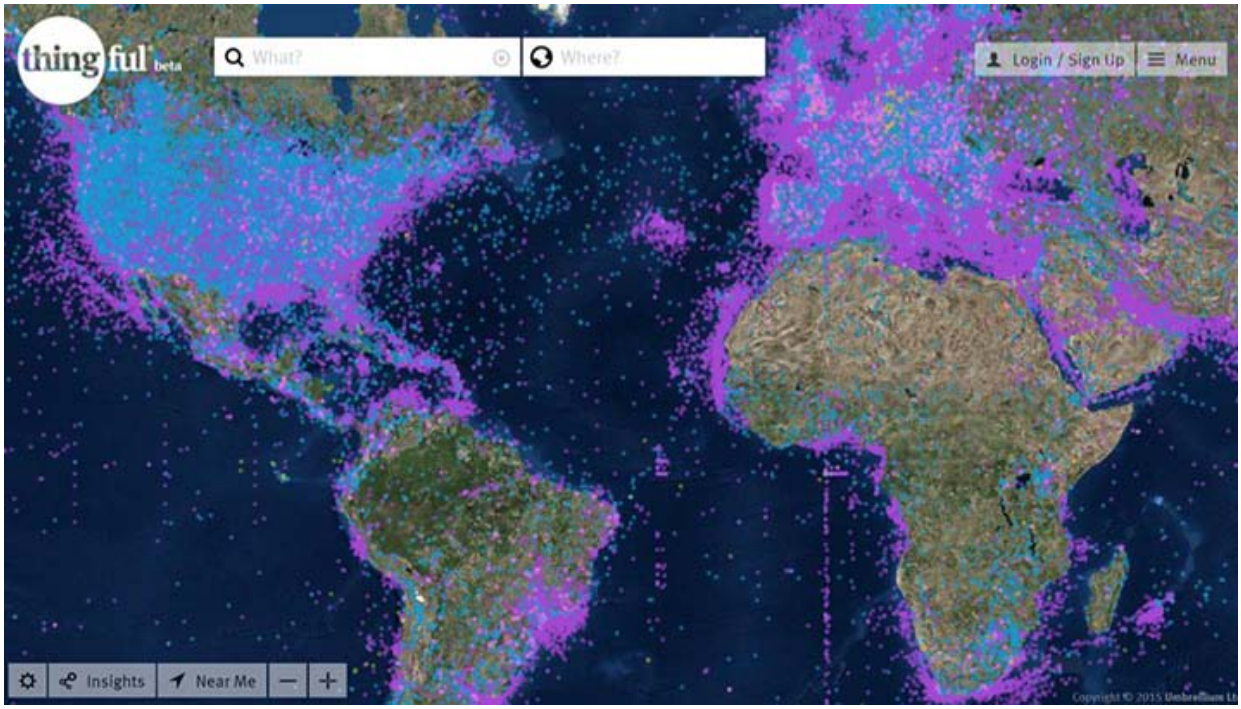
SENSORS IN THE IOT: Photonic sensing technology incorporates emission of light, transmission, deflection, amplification, and detection by optical components, instruments, lasers, other light sources, fiber optics, electro-optical instrumentation, and sophisticated nanophotonic systems. It provides smaller, cheaper, lighter, and faster components and products, with greater functionality while using less energy.

One might look at the IoT in the context of the internet evolving from a communication platform that provides access to information "anytime" and "anywhere" into a network that integrates "anything" by gathering and disseminating data from the physical world to enable a better understanding of our environment. The IoT allows us to make inferences about phenomena and take mitigation measures against unwanted environmental effects.

Photonics has been recognized as an enabling technology that impacts, extends across, and underpins a host of industrial sectors, from healthcare to security, manufacturing to telecommunications, energy to the environment, and aerospace to biotechnology. In all these sectors, photonics sensing activity can be recognized via the intelligent application of light either in an entirely novel context such as a new photodynamic medical treatment, or as a replacement to an older, outdated technology such as signage and lighting based on the use of incandescent lamps.

For example, the IoT fulfills all the technological requirements to be successful in developing countries: it is low power technology (good for places with unreliable power supply), it does not require a fast internet connection (nodes are sending small amounts of data, and servers can be local), it is low-cost (or getting there) and it has an immediate impact on people's lives. IoT applications can greatly benefit populations in developing countries: weather can be monitored, food safety can be checked, water quality can be analyzed, air quality can be measured, landslides can be detected and mosquitoes can be counted in cities in real time. Furthermore, cheap e-health kits can be shipped to the isolated areas of the developing world to bridge the healthcare gap between urban and rural settings. The picture below showing sensor nodes that

publish their data openly on the internet (https://www.thingful.net/) reveals a visibility gap where the North is scattered with nodes while the South is poorly represented. Africa, for example which is home to 1 billion people, has very few sensors.



Some interesting ideas have resulted from recently held workshops. In South Africa two students developed a pollution monitoring system to be installed on public buses. The system measures air quality and position via GPS, and sends the readings to a server via SMS. The air quality is visualized on Google Maps as shown in real time. In Kenya, a PhD student developed a low cost weather monitoring system to be used in rural areas. Building upon the training received in Cape Town in 2010, one of the participants from Malawi developed an irrigation system that reduces water consumption. From a workshop organized in Ghana emerged the idea of a joint project to develop an air pollution monitoring system including the effects of the Harmatan wind. The training in Thailand allowed researchers to study the effects of water temperature and oxygen on fish growth.

While high-end equipment is too expensive for hands-on training for scientists and engineers of the developing world, the emergence of off-the-shelf low cost sensor network equipment has enabled a new training model where knowledge is acquired on real devices. This model also allows scientists and engineers, both students and professionals, to be exposed to engineering design by having planning and configuration combined with fine-tuning of equipment during the training period to meet deployment requirements. The use of IoT will also enhance Computer Science curricula in academic institutions of developing countries. Long-term data from sensor networks will be valuable for educational purposes and the associated tools for curricula development should be encouraged.

While individual sensors may require minimal bandwidth, their aggregate contribution to the sea of IoT data may become quite large. As the problems tackled by IoT practitioners not just in developing countries, but around the world fall into categories (air quality, water quality, smart agriculture, healthcare, etc.), it is crucial that networks connecting IoT scientists & practitioners working in their domain be developed. The network will provide a way to harvest, store and communicate data for analysis and for researchers to share solutions and to collaborate on finding the best solution to their problem.

MEDICAL SENSORS

In addition to optical interconnects, several other applications are envisioned for silicon photonics. The technology can also play a role in biosensing applications. A disposable mass produced sensor would be attractive as it could grow the market for biosensors. Sensor applications are somewhat different from optical communication as there are other very low cost optical technologies that compete in this space. One likely application area for silicon photonics is the so-called lab-on-a-chip in which both reaction and analysis are performed in a single device. In the future, this could be extended to include electronic intelligence and wireless communications—key functions that will be needed to create intelligent sensor networks for environmental monitoring.

According to a report by Allied Market Research ("Global Photonic Sensors Market (Type, Technology, Application and Geography) - Global Opportunity Analysis and Forecast - 2013 - 2020"), the global photonic sensor market is forecast to reach $15.2 Billion by 2020, growing at a CAGR of 16.9% during the period (2014 - 2020). The study acknowledges the dominance of fiber optic sensors and sheds light on the way biophotonic sensors would garner more market share during the forecast period. Based on its application, biophotonic technology is expected to be the fastest growing technology in the photonic sensor market. Military is expected to be the largest revenue-generating segment until 2019, due to the wide-ranging applications of photonic sensors in various defense equipment. Geographically, North American region is leading and it would maintain the lead throughout the forecast period.

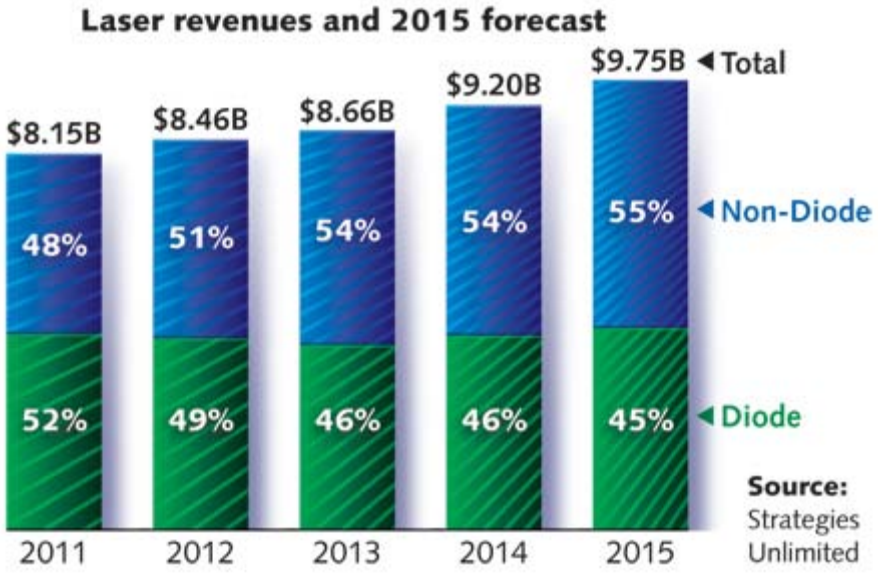
For we needle phobic patients, there is good news: scientists are discovering other, less invasive ways to see what’s going on inside the body – using tools such as light, lasers, fiber and integrated optical sensors without drawing blood. Researchers are now taking advantage of growing knowledge about how compounds like glucose absorb certain wavelengths of infrared light, for example, and using lasers to read them. A team at Princeton found a way to shine beams on people’s palms to get a relatively accurate reading of their blood-glucose levels, which could eventually spare diabetic patients frequent finger pricks.

Light is also being co-opted to treat disease. Photo-dynamic therapy relies on a drug that can be “activated” when exposed to specific wavelengths of light, making it ideal for treating tumors on the surface of organs or on the skin. In addition, borrowing from the world of micro-electronics, researchers are devising ways to use ultra-fine glass or plastic fiber optics to provide constant feedback on body readings, from things as simple as temperature to the presence of blood gasses like oxygen and carbon dioxide.

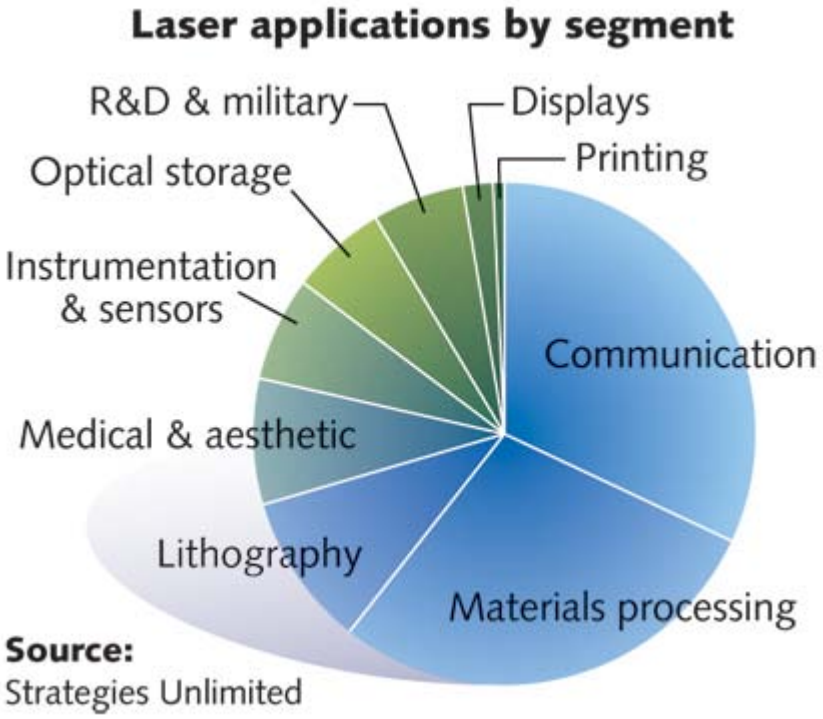
It may not be long before needles will be a thing of the past – for some tests anyway.

LASERS

Lasers literally surround us in our everyday lives and are finally being recognized globally and politically: first through the 50th Anniversary of the Laser events in 2010 and now through numerous global initiatives such as the United-Nations-decreed International Year of Light and Light-Based Technologies (IYL) in 2015.



The Strategies Unlimited in its report, "Worldwide Market for Lasers 2014" (www.strategies-u.com) indicates that most of the major laser manufacturing companies are definitely experiencing prosperity, with laser sales certainly exceeding low-single-digit, gross-domestic-product (GDP) growth rates. The communications and optical storage segment remains the largest in the laser industry, followed by materials processing and lithography lasers. And for 2014, medical and aesthetic laser sales totals continued to be larger than the instrumentation and sensors category, followed by the scientific research and military category.

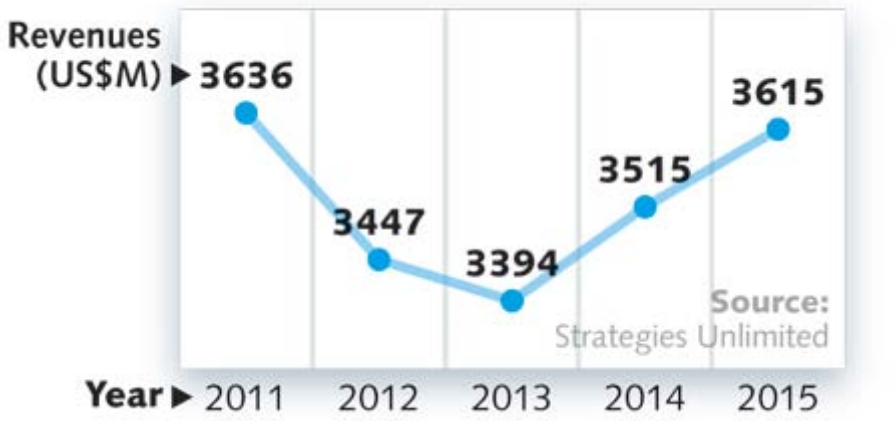


Laser diode and semiconductor optical amplifier (SOA) manufacturer Innolume (Dortmund, Germany) forecasts 2015 sales growth of between 25 to 30%, leveraging its product expertise in communications and medical markets. "Our biggest contributor to sales growth has been in medical applications, specifically, 1064 nm multimode laser chips for physiotherapy and a new biophotonic application for 2015 using tunable chips," says Innolume CEO Guido Vogel. "Having control over a vertically integrated laser diode manufacturing line from epitaxial growth to fiber coupling and supplying both quantum-dot and conventional quantum-well semiconductor laser chips and complete modules from 780–1320 nm positions us well for future growth. Our intense focus on sampling/prototyping activities with our customers over the past few years should bear fruit in 2015 and beyond."

In addition to biomedical instrumentation demand for chips and packaged devices, Vogel adds that data communications is an important future market for Innolume. "Our comb laser is a single-cavity DWDM [dense-wavelength division multiplexing] engine at 1310 nm able to power 8–16 channels of a datacom DWDM system and perfectly matches developments going on in the silicon photonics arena."

COMMUNICATIONS AND OPTICAL STORAGE includes all laser diodes used in telecommunications, data communications, and optical storage applications, including pumps for optical amplifiers. Communications and optical storage laser revenues reached $3.515 billion in 2014 and are forecast to grow around 2.8% to $3.615 billion in 2015. Despite glowing financials from most telecom laser providers in 2014, the Dell'Oro Group (Redwood City, CA) projects a telecom capital equipment expenditure drop in 2015, citing high mobile device penetration, slower mobile data growth, lack of new revenue streams, and increased competition from developed and

undeveloped markets. This forecast, however, is quite perplexing considering how the optical communications industry is promoting the IoT!



While 2013 and 2014 were relatively strong in the communications sector, there are signs that 2015 may be a bit slower. 100G has been the jumping point these last two years, driven in large part by wireless operators building up their backbones. Driving this on the device side, LTE and Wi-Fi networks continue to be deployed, and data traffic continues to grow.

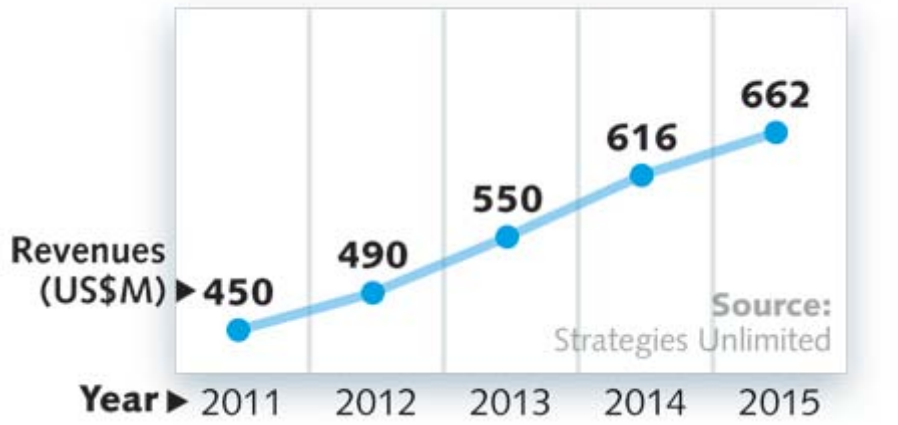
Prospects remain dim for optical storage. Streamed movies and music continues to grow in popularity, and solid-state memory prices continue to drop. Heat-assisted magnetic recording ("HAMR") or using lasers to increase storage capacity of magnetic media may have some commercial products by 2016 or 2017, but with the growing use of Cloud services by consumers, it is likely HAMR will only find use in some very specific niche server farm applications.

Optical storage weakness continues to damper overall laser sales in the communications and optical storage sector; however, communications laser sales are vigorous. PIC-based communications network system provider Infinera calls it the "Terabit Era" and reported sales growth to $174 million in Q3 2014 compared to $142 million in the same quarter last year. And LightCounting (Eugene, OR) said that global sales of optical transceivers reached $1.1 billion in Q2 2014, the fifth consecutive quarter of growth.

Whether you call it the IoT or simply a world of "smart gadgets" that will convert the driver's seat of an automobile into an Internet-connected data hub, it's fortunate that photonics—and lasers—are the "fuel" for this information engine. Can you imagine how much faster the Internet will need to operate in order to seamlessly manage the 4.9 billion connected devices that Gartner (Stamford, CT) says will be in use in 2015—up 30% from 2014—and forecast to reach 25 billion devices by 2020?

INSTRUMENTATION & SENSORS includes lasers used within biomedical instruments; analytical instruments (such as spectroscopy); wafer and mask inspection, metrology, levelers, optical mice, gesture recognition, LIDAR, barcode readers, and other sensors. The sensing arena, IoT applications and smart gadgets should keep laser manufacturers busy for decades to come. In addition, laser sales are benefiting directly from the U.S. oil and gas boom. Of the $585 million spent on distributed fiber-optic sensors in 2013 (and forecast to reach $1.46 billion in 2018),

70% of the sales are associated with the oil and gas market segments, according to the July 2014 Photonic Sensor Consortium survey published by Information Gatekeepers (Boston, MA). In the Strategies Unlimited forecast, the analytical, sensor, and life science instrumentation markets are expected to grow 7.5% to $662 million in 2015, surpassing the total laser sales for the combined scientific research and military market segments.



Laser instruments and sensors include a variety of applications that have become increasingly important in recent years. From lasers used in LIDAR for self-driving cars (see photonics in automobiles below), to lasers for flow cytometry and ultrafast spectroscopy for medical applications, the increasing processing power of today's microprocessors increasingly needs better sensors to supply data to be processed. When considering that laser revenue in this segment grew more than 12% in 2014, consider also that lasers used in this segment are also dropping fairly rapidly in price, which masks some of the real segment growth.

While some applications within this segment are flat or dropping in demand, such as lasers for barcode readers and laser PC mice, many others, such as gesture recognition for smartphones, are only in their infancy and could eventually amount to applications consuming millions of dollars of lasers. Overall, this is the segment to watch for some of the newest and most innovative laser applications.

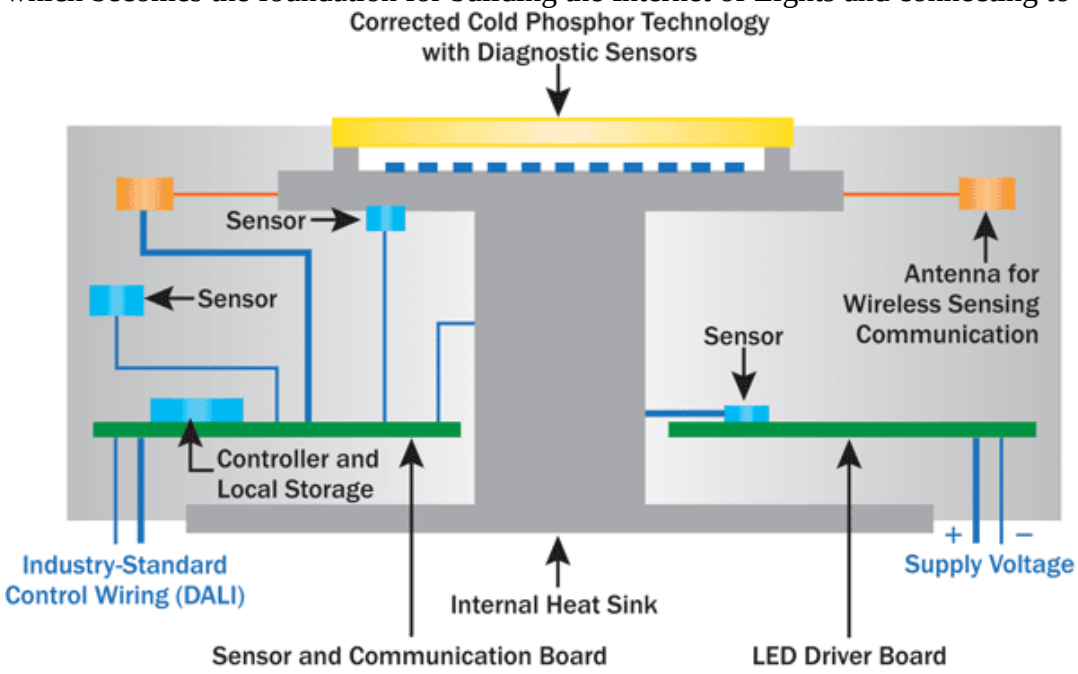
LIGHTING AND THE IIOT

Building-management, home-automation networks, Internet of Lights (enabled by the success of LEDs in lighting) and a variant of IoT - The Industrial Internet of Things (IIoT) at its simplest, can be defined as the integration of physical assets (machines, buildings, etc.) with sensors, control networks and intelligent software. The value propositions of the IIoT are analytics, remote access and management, collaboration, speed and accuracy of intelligence, and the easy capture and transfer of knowledge, not just data. The IIoT is much more demanding than the consumer or human Internet of Things, which is characterized by applications and functions that involve human interaction such as wearable fitness trackers or home thermostats. The more stringent requirements of the IIoT include:

- Autonomous control, or the ability to operate without human intervention – either because the industrial environment is somehow inappropriate for people or because actions must take place too quickly, frequently or reliably to be handled by people.

- Peer-to-peer operation, without interaction with an Internet server or cloud.
- Industrial-strength reliability and industrial-grade security.
- Support for wired as well as wireless connectivity.

An Internet of Lights is formed when all the smart lights in a space are connected by digital networks and are able to communicate with each other, communicate with a server or gateway, and communicate with sensors and controls in proximity of the lights. In such a configuration, the Internet of Lights becomes the backbone of a building-management or home-automation network. What makes this really attractive is that lights are virtually everywhere, and they already have (electrical) power to the light itself. This power can be used to run other electronic components and devices integrated into, or attached to, the networked lights. Like LED lighting, almost all electronic components used for communication, control and sensors are also low-voltage components that can share the same power supply, reducing the component count and costs. The figure below ('Internet of Lights' Meets Industrial Internet of Things - Gerard Harbers, Xicato, and Sanjay Manney, Echelon Corp) shows the components of the intelligent module, which becomes the foundation for building the Internet of Lights and connecting to the IIoT.



Sensors and controls can be directly attached to the lights and the Internet of Lights network, or can also be incorporated via short-range wireless connectivity options, such as 6LoWPAN or Bluetooth Smart radios. In this way, the lights become access points for the IoT, where the "things" could have short-range wireless radios with very long battery life due to the proximity of the access points. Hence, as individual lights become smarter and then are networked together and connected to additional sensors, actuators and other devices ***the Internet of Lights meets the Internet of Things – a new world of opportunities is likely to be created.***

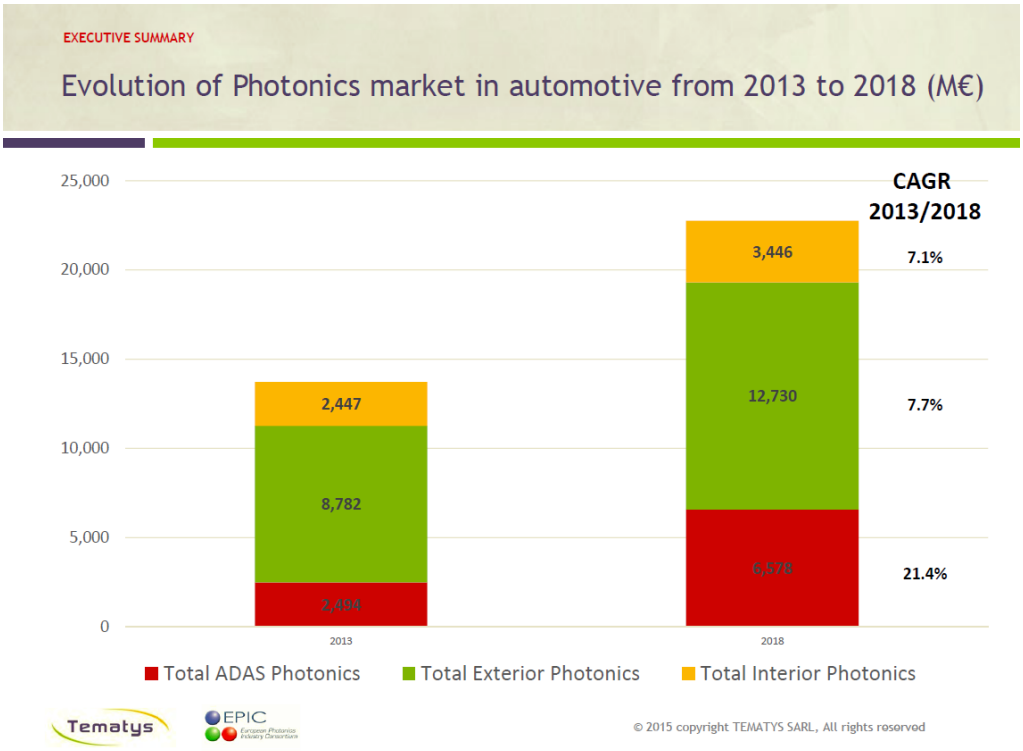
Photonics in automobiles

Photonics in automobiles and the trend toward innovation is a huge opportunity for the photonics industry. It allowed and will continue to allow new photonic technology to enter the car. According to a study from the NHTSA (National Motor Vehicle Crash Causation Survey, NHTSA, 2008 - National Highway Traffic Safety Administration, USA), human error is the critical reason in around 90% of all car accidents. Hence the automation of certain driving tasks would help reduce the human error factor and so the number of car crashes. It is the reason why Advanced Driver Assistance Systems (ADAS) are implemented in cars. Adoption of ADAS is required to reach the goal of a continuous decrease in fatality rates on the road and photonics is a key enabler of active safety functions. Photonic technologies are especially good at sensing the environment, which is critical for driving assistance applications. Consequently, photonic technologies are expected to be widely adopted in ADAS, explaining the high growth of Photonics in ADAS applications.

The production of cars worldwide is expected to almost double in 20 years (Tematys), from 56 million of cars produced in 2000 to around 105 million forecasted in 2020. The **ADAS segment,** embodying systems that help the driver with the driving process, are also called active safety systems. Photonic technologies have different functions that cover several applications of active safety:

- Imaging and Sensing (outside/inside): cameras or LIDARs for sensing and imaging the car surroundings
- Lighting: intelligent headlights
- Communication: optical car-to-X communication
- Display / HMI: head-up displays

Cost decreases, while retaining high performance, makes photonics attractive for the automotive industry. Other applications include: parking assist, lane keeping assist, automatic emergency braking, adaptive cruise control, blind spot detection, traffic sign recognition, night vision systems, and adaptive front lighting.



Today the only photonic technologies with an adoption superior to 10% are optical components. Other photonic technologies are still too expensive and are mainly adopted in luxury level cars.

Technology: © Tematys	2013	2014	2015	2016	2017	2018	2019	2020	$CAGR_{2014-2020}$
Optical Components	221	235	247	253	258	260	273	281	22%
Cameras	1000	1130	1266	1582	1978	2492	3040	3648	23%
Communication	20	21	25	30	39	51	72	100	21%
AFS**	685	757	739	1104	1496	2000	2348	2646	3%
LIDAR	42	48	57	68	82	101	123	151	23%
Night Vision	112	162	215	287	396	454	523	567	30%
HUD*	414	489	596	763	976	1221	1526	1680	23%
Total	2494	2842	3145	4087	5226	6578	7904	9073	22%

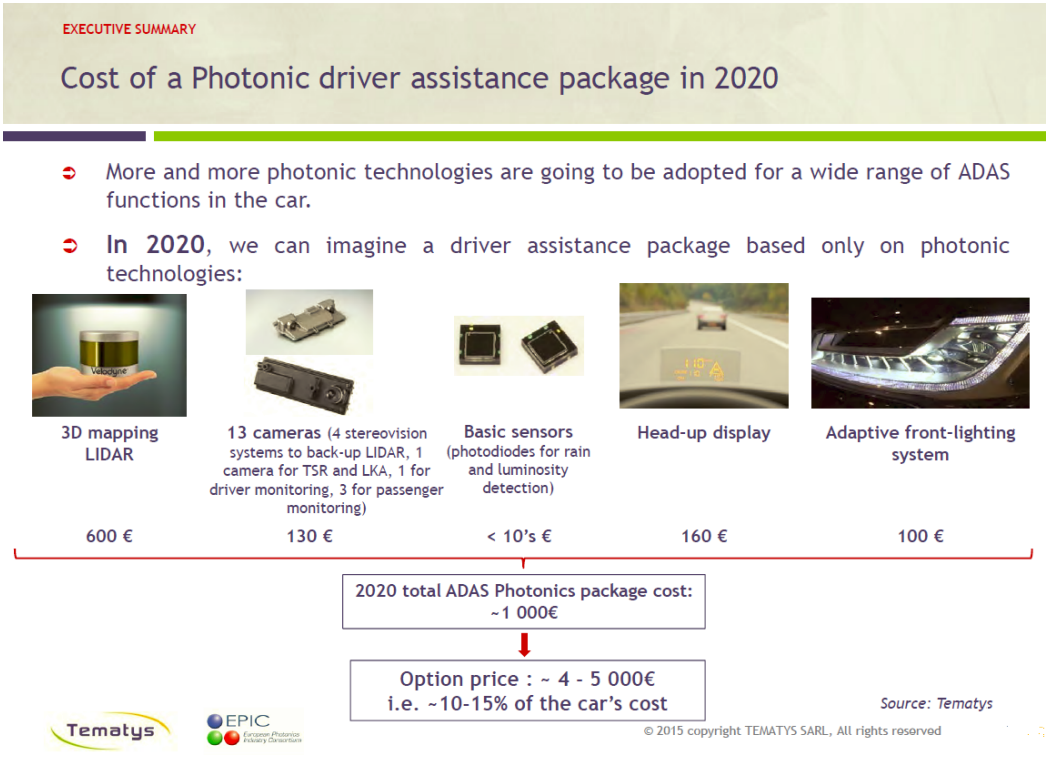
The market of Photonics in ADAS is expected to grow from around $2.8 b in 2013 to >$10 b in 2020. The highest growth markets are predicted to be adaptive front lighting systems followed by cameras and head-up displays.

Technology: © Tematys	2013	2014	2015	2016	2017	2018	2019	2020
Optical Components	246	261	275	302	323	352	389	401
Cameras	25	32	42	63	99	166	253	365
Communication	0,02	0,02	0,03	0,1	0,2	0,5	0,9	1,7
AFS**	4,2	4,7	5	9	14	20	25	29
LIDAR	0,04	0,05	0,07	0,1	0,2	0,24	0,4	1
Night Vision	0,2	0,4	0,7	1	3	4	5	6
HUD*	2,0	2,4	3	4	5	7	9	11
Total	277	301	326	380	445	550	683	814

The total number of photonic technologies sold for ADAS applications was around 300 million in 2013. It is expected to surpass 800 million units in 2020. Optical components represent the highest volume but not the highest revenue as, in this sector, they are very low cost devices.

The market of Photonics in Automotive is $15.3 b in 2013 for ADAS, interior and exterior applications.

- This market is expected to grow at a fast CAGR of 10.6.%, 2.5 fold the growth of the automotive light vehicles market (4.1%). It will reach $ 25.4 b in 2018.
- In 2013, the core business remains Lighting which accounts for 72% i.e. $11 b.
- However, with a CAGR of 21.4 %, the ADAS segment is the fastest growing market in the next 5 years (5 fold the average automotive market). It is expected to grow from $2.8 b to $7.4 b in 2018.



As shown the above figure, automotive adoption is strongly related to cost. Indeed, even a system with acknowledged added-value has to get below a certain cost to enter mainstream cars. Basic optical components achieved a wide adoption because there cost decreased below $1. As a comparison, HUD and AFS currently cost over $168 and night vision systems or LIDARs cost over $560. Therefore, the first objective of photonic technologies is to target luxury and premium segments. Then, to reach medium and entry level cars a technological breakthrough is needed to divide price by 10 or 100.

Technologies that are going to be easily adopted in the short term (before 2020):

- Cameras for inside and outside monitoring: cheap and can be used for several applications
- Head-up displays: added-value is immediate for the customer
- Adaptive front lighting systems: high added-value and cost decrease due to LED cost decrease

Technologies that are going to be adopted in a longer term: LIDARs: the main barrier for the wide adoption of high-end photonic technologies such as 3D mapping LIDAR is their high costs. Their adoption rate will be weak until 2020 and is expected to grow faster in the next decade. Indeed, technological breakthrough will be needed for automated tasks in complex situations (in town).

Technologies that will not be adopted easily:

- Night vision systems: the added-value over price ratio is too low
- Optical communication for V2V and V2I communication: massive lobby of Wi-Fi

Transition is not only about manufacturing & sales but innovation content too. The automotive industry has long been a traditional industry. However, for the last 10 years car manufacturers have demonstrated increasing interest in new technologies in all areas: lighting, powertrain, driver assistance and more. Consequently, in 2013, it has become one of the most innovative industries according to a survey (The most innovative companies 2013, BCG) from the Boston Consulting Group with annual investments over $94 billion in research, development and production (Source OICA website). Indeed, 14 automakers are among the 50 most innovative companies, and three are in the top 10: Toyota, Ford, BMW. Moreover, the survey shows that carmakers place innovation as one of the top priority in their strategy.

ROADMAP OF QUANTIFIED KEY ATTRIBUTE NEEDS (2015 – 2025)

Following are a partial list of quantified key attributes extracted from the Portable Systems Product Sector chapter of the iNEMI 2015 Roadmap. In addition we have attempted to include specific key attributes unique to integrated photonics.

Roadmap of Quantified Key Attribute Needs (2015 – 2025)

Parameter	Metric	*2013*	*2015*	*2017*	*2019*	*2025*
PCB Costs						
2 layer flexible	$ per cm2	0.025	0.020	0.015	0.010	0.005
2 layer Rigid	$ per cm2	NA	0.0063	0.006	0.0058	0.005
3 layer flex	$ per cm2	NA	NA	NA	NA	NA
6 layer flex (with micro vias)	$ per cm2	0.065	0.050	0.040	0.025	0.013
4 layer conventional	$ per cm2	0.020	0.008	0.008	0.008	0.008
4 layer - embedded capacitor / resistor	$ per cm2	NA	NA	NA	NA	NA
6 layer conventional	$ per cm2	0.025	0.013	0.012	0.012	0.010
4 layer w/ microvia	$ per cm2	0.040	0.0274	0.0247	0.022	0.018
6layer rigid (with micro vias)	$ per cm2	0.065	0.050	0.040	0.030	0.020
6 layer, blind/buried	$ per cm2	0.085	0.070	0.055	0.035	0.025
8 layer	$ per cm2	0.040	0.016	0.015	0.015	0.012
8 layer w/ microvias	$ per cm2	0.080	0.044	0.040	0.036	0.028
8 layer w/ blind/buried	$ per cm2	0.100	0.080	0.065	0.040	0.030
8 layer colaminated (ALIVH)	$ per cm2	0.120	0.100	0.080	0.050	0.035
10 layer conventional	$ per cm2	0.050	0.028	0.027	0.026	0.020
10 layer w/ microvias	$ per cm2	0.120	0.053	0.046	0.042	0.030
10 layer w/ blind / buried	$ per cm2	0.140	0.120	0.100	0.070	0.038
10 layer colaminated (ALIVH)	$ per cm2	0.140	0.120	0.100	0.070	0.040
Assembly Costs	#REF!					
Average Board Assembly Cost	¢ per I/O	0.035	0.02	0.02	0.01	0.006
Average Final Product Assembly Cost	$/unit	1.15	1.05	0.98	0.9	0.5
Package Costs	#REF!					
IC Package Cost	¢ per I/O	0.15	0.1	0.1	0.08	0.05
Package Cost (High Density Ceramic/w/ Area Connector)	¢ per I/O	0.6	0.5	0.4	0.2	0.1
Package Cost (High Density µvia Laminate w/ Area Connecto	¢ per I/O	0.03	0.025	0.2	0.1	0.05
Connector Cost	¢ per I/O	0.005	0.004	0.003	0.002	0.001
Energy Cost	$/Wh	0.4	0.3	0.25	0.2	0.1
Memory Cost (Flash)	$/MB	0.03	0.015	0.007	0.004	0.002
Memory Cost (SRAM)	$/MB	0.85	0.7	0.55	0.4	0.2
Cost of Test as a ratio to assembly	ratio	0.025	0.02	0.015	0.01	0.005

Parameter	Metric	2013	2015	2017	2019	2025
PCB Costs						
2 layer flexible	$ per cm2	0.025	0.020	0.015	0.010	0.005
2 layer Rigid	$ per cm2	NA	0.0063	0.006	0.0058	0.005
3 layer flex	$ per cm2	NA	NA	NA	NA	NA
6 layer flex (with micro vias)	$ per cm2	0.065	0.050	0.040	0.025	0.013
4 layer conventional	$ per cm2	0.020	0.008	0.008	0.008	0.008
4 layer - embedded capacitor / resistor	$ per cm2	NA	NA	NA	NA	NA
6 layer conventional	$ per cm2	0.025	0.013	0.012	0.012	0.010
4 layer w/ microvia	$ per cm2	0.040	0.0274	0.0247	0.022	0.018
6layer rigid (with micro vias)	$ per cm2	0.065	0.050	0.040	0.030	0.020
Cycle Time						
NPI Cycle Time	Weeks	14	12	10	6	4
Product Production Life (not including spares)	Years	3	3	3	3	3
Reliability						
Temperature Range	Deg C - Deg C	-40 - +85	-40 - +85	-40 - +85	-40 - +85	-40 - +85
Number of Cycles	Cycles to Pass	manuf spec	manuf spec	manuf spec	manuf spec	manuf spec
Vibrational Environment (PWB level)	G^2/Hz	UA	UA	UA	UA	UA
Use Shock Environment	Gs & ms to Pass	20G(20ms)	20G(20ms)	20G(20ms)	20G(20ms)	20G(20ms)
Devices	#REF!					
Number of stacked die (Max)	#	8	10	11	12	20
Sensors	Types	Gyro, Accel, GPS	revious plus Haptic	amera, Context Camera (gesture recognition)		
Number of Die in SiP (max)	#	5	5	6	7	12
Maximum MEMS Power Consumption	W					
MEMS	Types	Gyro, Accel, GPS	Gyro, Accel, GPS	prev+projection	prev+projection	prev+medical
Max. Ohms	ohms / sq. cm	10K	100K	100K	100K	100K
Max. Capacitance	µF / sq. cm	10K	250	500	700	1000
Min. % tolerance	%	10	5	5	2	1
RF Components						
Quality Factor	Q	20	125	400	1000	5000
Capacitance density	nF/sq. cm	0.3	1	10	100	500
Inductance req.	nH	15	30	300	1000	1000
Interconnect Insertion loss maximum	db/cm/GHz	0.05	0.008	0.0025	0.001	0.0002
Photonic Components						

Parameter	Metric	2013	2015	2017	2019	2025
Memory						
Main Memory Type	Type	SRAM	Stack D&S	eDRAM, NVM	eDRAM, NVM	eDRAM, NVM
Main Memory Capacity	MB	256	1 GB	5 GB	10 GB	100GB
Storage Type	Type	Card/Slot	Disk	Disk?	Optical ?	Optical
Storage Capacity	MB	5 GB	20 GB	100 GB	500GB	1TB
Maximum Power	mW					
Minimum Speed	GB/sec					
Components/ Package						
Max Component I/O density	I/O/sq.cm	500	600	700	800	1200
Average Component I/O density	I/O/sq.cm	50	55	60	80	120
Average Component Density	#/sq.cm	30	40	50	80	120
Maximum I/O per package	I/O per part	600	675	725	1000	1400
Average I/O per package	I/O per part	7	7.5	8	9	11
Max Components/sq. cm.	#/sq.cm	55	60	70	75	95
Max I/O for 50 mm square SCM w/ full area array	#	3000	3500	5000	8000	1300
Package I/O Pitch, (area array)	mm	0.4	0.4	0.3	0.3	0.3
Package I/O Pitch for SCM (area array)	mm	0.4	0.4	0.3	0.3	0.3
Package I/O Pitch for MCM (area array)	mm	0.5	0.4	0.4	0.3	0.3
Package I/O Pitch (perimeter)	mm	0.4	0.4	0.3	0.3	0.3
Number of Terminals - Max Digital	#	600	675	725	1000	1400
Number of Terminals - Max RF	#	100	150	200	350	600
Maximum Component Height	mm	1.0 to 2	1.0 to 1.5	0.7 to 1.2	0.4 to 1.0	0.2-0.5
Maximum Body Size (L x W)	mm	38	40	42	50	50
Minimum Terminal Pitch BGA	mm	0.4	0.4	0.3	0.3	0.3
Minimum Terminal Pitch Leadless	mm	0.4	0.4	0.3	0.3	0.3
Minimum Component size (LxW)	mm	0.5	0.5	0.4	0.3	0.3
PCB / Substrates						
PCB Board Size (Min)	sq. cm	0.75	0.5	0.3	0.2	0.1
PCB Board Size (Max)	sq. cm	80	64	52	40	30
Substrate Lines/Spaces	µm	65	65	50	35	20
Substrate Pad Diameter	µm	175	150	125	100	50
Ceramic Thin Film Lines/Space	µm	35	25	20	10	5
PCB Land Diameter With Vias for BGA - Via in Pad (VIP)	µm	300	250	200	150	100
PCB Minimum Plated-thru-via (PTV)	mm	0.15	0.1	0.1	0.075	0.05
Substrate Material	Type	FR4	FR4	FR4	FR4	FR4
PCB Lines And Spaces	µm	300	300	250	250	200

Parameter	Metric	2013	2015	2017	2019	2025
Electrical & Test						
Frequency on Board	MHz	250	300	350	400	500
Impedance Tolerance	%	10	10	5	5	1
Built In Self Test (BIST)	%	50	70	85	90	90
Boundry Scan	%	20	35	50	75	90
Minimum Logic Family Voltage	Volts	2	1.8	1.5	0.8	0.7
Maximum Logic Family Voltage	Volts	3.3	2.85	2.2	1.8	1
Normal Logic Family Voltage	Volts	2.85	2.2	1.8	1.2	0.8
Test pad access minimum	%	25	20	10	5	5
Minimum test pad size	mm²	1	1	0.8	0.7	0.5
Maximum escape rates	DPMO	1000	500	200	100	100
Power	#REF!					
Power	Type	u Polymer, methanol	u Polymer, methanol	u Polymer, methanol	u Polymer, methanol	u Polymer, methanol
Spec. energy	Wh/kg	120	150	200	250	500
Energy dens	Wh/liter	138	150	230	300	500
Cycle life	#cycles-80%	1000	1200	1500	1800	2000
Specific power	W/kg	300	400	500	600	1000
Shelf life	years	3 years	4 years	5 years	8 years	10 years
Run Time Before Recharge	Hours	8	10	15	20	40
Min. and Max. Operating Temperature	Degrees C	-20 to 30	-25 to 35	-30 to 40	-30 to 45	-40 to 50
Battery Cost (Maximum)	$/Wh	0.6	0.5	0.4	0.2	0.1
Battery Recaharge Time (Maximum)	Hours	4	3	2	2	1
Environmental						
Minimum MSL Level	Level #	3	3	2A	2A	2
Max Reflow Temp	Degrees C	260	260	260	260	220
Solder Type	Composition	LF	LF	LF	LF	LF
Hazardous Substance Content	% by weight	0	0	0	0	0
Recycling targets - Recovery, Recyclability	%,%	70/60	75/65	80/70	95/90	95/95
Thermal						
Use Ambient Operating Temperature Range	Deg C - Deg C	-10 to 50	-10 to 50	-10 to 50	-10 to 50	-10 to 50
Thermal Design Power (Hottest Chip)	Watts	40	45	50	60	60
Cooling Method	Passive,Active, None, Both	both	both	both	both	
Number of Chips W/Some Heat Sink	# / Assy or Board	0	0	0	0	0
Device Cooling Air Temperature (Inside the Box)	Deg C	40	40	40	40	40

CRITICAL INFRASTRUCTURE ISSUES

IDENTIFY PARADIGM SHIFTS

The IoT – so what can we do that we couldn't do before? Well, users have, in a significant way, taken control of information! As an increasing number of devices are being connected to the Internet, information is evolving from what we know today into a whole new mindset where continuous development and modular authoring is paramount. The production of technical information has for many decades been a fairly routine process. Products are manufactured, documented and marketed, and when they are being sold, the printed documentation is handed over to the owner or gets distributed to service technicians.

With the evolution of the Internet, a paradigm shift began, directing information to displays and less towards printed media. Handbooks are being replaced by apps and user web forums, information about repair and maintenance procedures became available via service portals, accessories and parts systems are digitally distributed and connected to e-commerce websites and business platforms. In addition, a company's product information today is primarily competing with social channels such as Youtube, Wikipedia and Ifixit among others. The users have taken control of the information.

The IoT introduces another paradigm shift and encapsulates the notion that information will likely be completely integrated into products – information content has become an inextricable part of the product itself! The challenge for us – the information authors - to continuously describe the components of ever-changing products. Connected things bring new value – all sorts of things as noted earlier - because connected things can intelligently make use of each other in order to make the human life easier and more efficient.

From "**Smart Dust**" systems that can be embedded (and even **ingested**) all the way to the satellites driving an **Interplanetary Internet** system. The range of hardware devices that will drive an Internet of Things is staggering! IoT will create new winners long before losers find out they're losing.

TECHNOLOGY REQUIREMENTS AND TRENDS

IoT isn't coming soon - it's already here! A typical car produced in 2014 has between 60-100 built-in sensors. The IoT connects the physical world to the Internet. The IoT connects billions of sensors and devices such as every day consumer objects and industrial equipment onto networks. Networked inputs are then combined into bi-directional systems for better decision making, increased efficiency, new services, or environmental benefits. Increasing amounts of data produced by those sensors and connected devices are hence acquired, logged, and stored onto networks. And although the IoT IS already here – but it is not evenly distributed!

The IoT paradigm, while not evenly distributed yet, IoT is already here, rapidly connecting the physical world to the Internet. IoT is inevitable, affecting every industry, every company, every job, and every person. IoT is going to be huge. 212 billion devices will be part of the IoT by 2020 (Samsung IFA 2014 / International Data Corporation (IDC), 2014). IDC predicts that IoT will generate nearly $9 trillion in annual sales by 2020. Not convinced? Within 6 years, 57,000 new "things" will be added to the Internet every second. For businesses, IoT requires a mindset shift because it will create and capture value differently. IoT is both a driver of new product cycles and another leg of cost efficiencies. Products can address needs in a predictive manner, leveraging data and frequent updates. IoT enables incremental revenue, control points and opportunities for partnerships in the ecosystem. IoT will create new winners long before losers find out they're losing. It is necessary to understand and leverage this evolution, so that we can face the requirements that will be placed on us, as well as benefit from all the opportunities it creates.

Truly, the sky is the limit in terms of IoT applications.

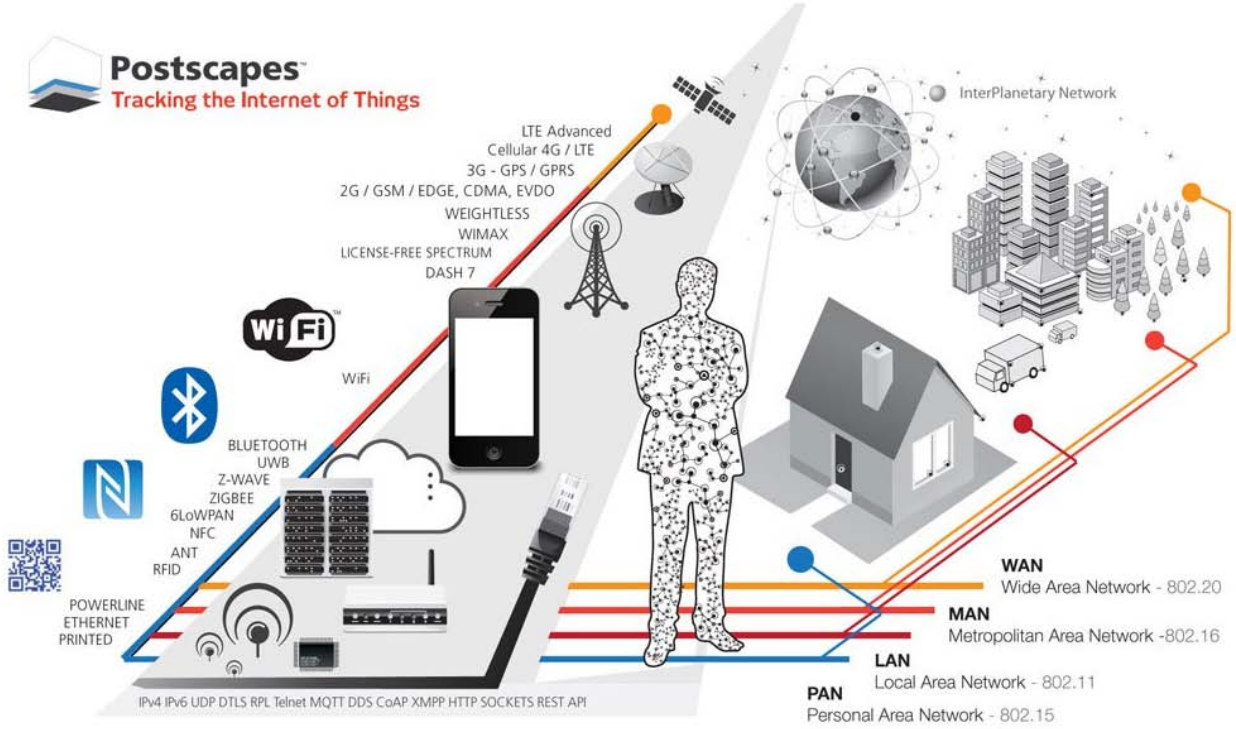
- Home consumer: Thermostats, Lighting, Remote control appliances, Detection (intrusion / smoke), Energy / water monitoring, Infotainment, Pet feeding
- Health & Body: Patient care, Patient surveillance, Elderly monitoring, Fall detection, Remote diagnostic, Equipment monitoring, Hospital hygiene, Bio wearables, Food sensors
- Cities & Industry: Smart lighting, Waste management, Maintenance, Surveillance, Signage, Utilities / Smart grid, Emergency services
- Transportation & Mobility: Smart car, Traffic routing, Telematics, Package monitoring, Smart parking, Insurance adjustments, Supply chain, Shipping, Public transport, Airlines Trains
- Buildings & Infrastructure: Heat, ventilation and air conditioning, Security, Smart lighting, Transit, Emergency alerts, Structural integrity, Occupancy, Energy credits

IoT revenues predictions are staggering in every category (Source: IDC - Internet of Things Spending Guide by Vertical Market, 2014):

• BANKING:	2014: $92B	2018: $154B
• MANUFACTURING:	2014: $472B	2018: $913B
• RETAIL:	2014: $160B	2018: $326B
• HEALTH:	2014: $132B	2018: $313B

- TRANSPORTATION: 2014: $156B 2018: $325B
- UTILITIES: 2014: $100B 2018: $201B
- GOVERNMENT: 2014: $301B 2018: $570B
- OTHER: 2014: $750B 2018: $1.78T

http://postscapes.com/internet-of-things-technologies#communication



TECHNOLOGY CHALLENGES

Connectivity/Signaling: There will not be one connectivity standard that "wins" over the others. There will be a wide variety of wired, wireless and free space photonic standards as well as proprietary implementations used to connect the things in the IoT along with and connectivity via data centers required to collect, process and distribute the information. The challenge is getting the connectivity standards to talk to one another with one common worldwide data currency. With connected IoT devices, reliable bidirectional signaling is essential for collecting and routing data between devices. That's where IoT data streams comes into play. Devices may be talking to a server to collect data, or the server may be talking to the devices, or maybe those devices are talking to one another. No matter what the use case, data needs to get from point A to point B quickly and reliably. You need to be 100% sure that that stream of data is going to arrive at its destination every time.

Security: With the amount of data being sent within the IoT, security is a must. Built-in hardware security and use of existing connectivity security protocols is essential to secure the

IoT. Another challenge is simply educating consumers to use the security that is integrated into their devices. Remember - 50 Billion Connected Devices by 2020 Security is a huge umbrella, but it's paramount in IoT connectivity. For example, what good is a smart home if anyone can unlock your doors? Here are three specifics:

- Authorization: When sending or receiving a stream of data, it's essential to make sure that the IoT device or server has proper authorization to send or receive that stream of data.
- Open ports: An IoT device is dangerously vulnerable when it's sitting and listening to an open port out to the Internet. You need bi-directional communication, but you don't want to have open ports out to the Internet.
- Encryption: You need end to end encryption between devices and servers.

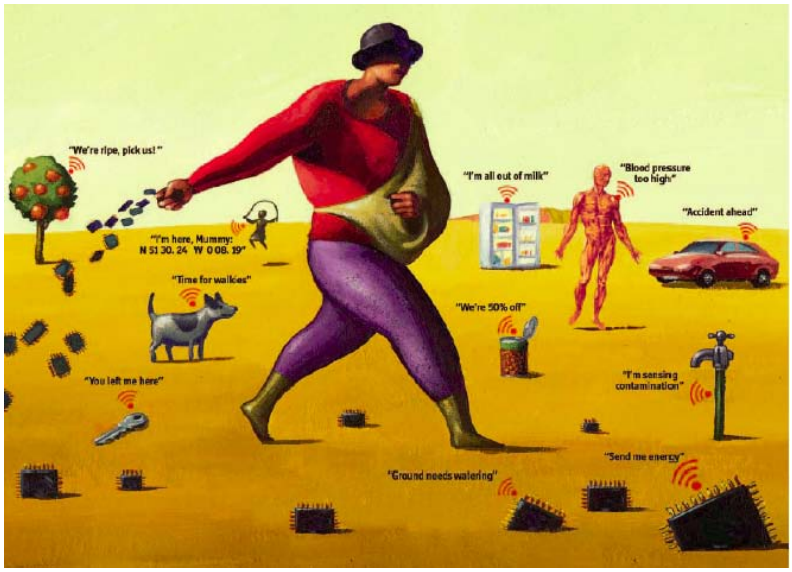
Power management: Billions of IoT devices signaling and sending data between one another takes a toll on power and CPU consumption. More things within the IoT will be battery powered or use energy harvesting to be more portable and self-sustaining. Line-powered equipment will need to be more energy efficient. The challenge is making it easy to add power management to these devices and equipment. With all this communication, you need minimal battery drain and low power consumption and wireless charging will incorporate connectivity with charge management.

Complexity: Manufacturers are looking to add IoT connectivity to devices and equipment that has never been connected before. Ease of design and development is essential to get more things connected. The average consumer needs to be able to set-up and use their devices without a technical background. Presence detection will also play a role here. It's important to immediately know when an IoT device drops off the network and goes offline. And when that device comes back online, you need to know that as well. Presence detection of IoT devices gives an exact, up to the second state of all devices on a network. This gives you the ability to monitor your IoT devices and fix any problems that may arise with your network.

Bandwidth: In addition to power and CPU, bandwidth consumption is another challenge for IoT connectivity. Bandwidth on a cellular network is expensive, especially with hundreds of thousands of IoT devices on a network sending request/response signals to your server. That's a huge server issue and requires a large scale server farm handling all this data. You need a lightweight network that can seamlessly transfer data between devices and servers.

Internet of Things Architecture: In the near future, these billions of devices connected IoT will include sensors and actuators in smart cities, smart tags on many familiar objects, wearable health monitoring sensors, smartphones, intelligent cars, and smart home appliances. In the not so distant future, IoT will incorporate many types of robots like domestic, flying drones, and even insect scaled flying devices. The changes to our daily life will be immense. *Today's* technology isn't ready for this massive scale and the highly dynamic nature of the future IoT, the huge amounts of data streamed from the physical world, and the new communication patterns it will create. We need new programming, network management and content delivery approaches that is realized with a systems engineering approach – integrated hardware, software, networking, powering…all talking together from the inception. Today's IoT architectures were

designed for small scale IoT closed-looped network "islands" using proprietary protocols. Densely deployed "things" can't collaborate dynamically across these islands to execute distributed tasks that involve sensing, actuating, and computing. *We need to break down the technology silos and create a flexible, event-driven architecture that allows seamless data sharing among applications.*



Vivid image of the IoT by Jon Berkeley – *The Economist*, 2007

Silicon Photonics: With so many things connected to Internet, however, there is increasing demand for more network traffic, especially higher capacity in core networks. In addition, the shaping of IoT is largely depending on technologies like Internet Protocol version 6 (IPv6), cloud computing, Internet everywhere, and sensors. Most of these technologies are also asking for high capacity network traffic. In the end, it's all about bandwidth and using technologies and products that can achieve higher network traffic capacity and the desire for higher levels of integration of optics favors the adoption of silicon photonics. The system level cost management, integration density, and power limit trade-offs must be carefully considered as development of silicon photonics is pursued.

- Speed & High Bandwidth: Optically transmitted signals run over long distances and at high signal rates superior to any other media - one big obstacle to IoT.
- Security: Optical networks are the most secure and hack-proof - another big obstacle to IoT.
- NO Electromagnetic Interference - making optical interconnects a number one choice for IoT's network.

CONCLUSIONS

The IoT is expected to continually change and evolve – rapidly! More devices are being added every day and the industry is still in its infancy. Many of the challenges facing the industry are yet unknown. Unknown devices. Unknown applications. Unknown use cases. Given this, there

needs to be flexibility in all facets of development. Processors and microcontrollers that range from 16–1500 MHz to address the full spectrum of applications from a microcontroller (MCU) in a small, energy-harvested wireless sensor node to high-performance, multi-core processors for IoT infrastructure. A wide variety of wired, wireless and photonic connectivity technologies are needed to meet the various needs of the market. A wide selection of sensors, mixed-signal and power-management technologies are required to provide the user interface to the IoT and energy-friendly designs.

The new technologies that are becoming available must meet these challenges– complexity, connectivity, security, bandwidth, power, and environmental. Key, new processor packaging technologies are being developed with some fundamental changes in the rest of the electronics industry and how it impacts the technology that can be leveraged. With the IoT, a new set of technology will evolve, but often at a much different scale of size, bandwidth and latency than required by typical data centers.

REFERENCES AND ACKNOWLEDGEMENTS

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PSMC DATA CENTER PRODUCT EMULATOR

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PSMC DATA CENTER PRODUCT EMULATOR

EXECUTIVE SUMMARY

The Data Center Product Sector Emulator covers the technologies that enable high-performance computing systems, data centers, and communications systems. The data explosion generated by the growth in social networks and digital entertainment, cloud-computing, and IoT are radically driving the growth of data centers and the need for high bandwidth, low-latency communications.

These forces are transforming the data center structures to a higher level of integration of computing, storage and networking components. The data bandwidth demand is resulting in systems with ever faster interconnect speeds, even as processor speed is staying constant. The size of the data centers creates a challenge for power demand creating an increasing focus on power efficiency of the systems. The data centers have an increasing number of systems residing in an environment of higher temperature, humidity and corrosive elements to reduce the operation costs and manage the total cost of ownership of these systems. Achieving this rapid growth places increasing demands on increasing the performance and decreasing the cost of next generation equipment. Because of the capital requirements for adding capacity, all segments are undergoing rapid consolidation and movement to external cloud services.

The industry analysis by IHS projects a factory OEM revenue growth of 4.4% CAGR over the next 10 years from a cumulative $162B today to $273B in 2025. The growth in the Data Center sector is particularly strong, growing from $7B today to $22B in 2025 driven by the rapid increase in data traffic. The rate of innovation in the Data Center sector is high, enabled in part by the open source concepts of hardware and software. The Enterprise Communications sector is still recovering from the economic meltdown of 2008-2009 and upgrades are slow. However metro networks are heavily utilized, with the proliferation of 4G and investments including 100G interconnect. The Service Provider Equipment is more closely tied to short term economic trends and forecast growth of 5.4% CAGR is driven by technology upgrades and convergence.

The assembly and packaging technology to support the data centers continues to advance. In particular the need for high-speed, low-latency data transfer is driving the need for integrated silicon photonic components. The enabling technologies include:

- **Heterogeneous packaging** (Through-Silicon Vias (TSV) for stacked chips and silicon interposers,
- System in Package (SiP) and Package on Package (PoP)),
- **integrated silicon photonics systems**,
- lower loss interconnect (low-loss laminates in printed circuit boards and packages,
- More efficient power conversion (wide band-gap materials).

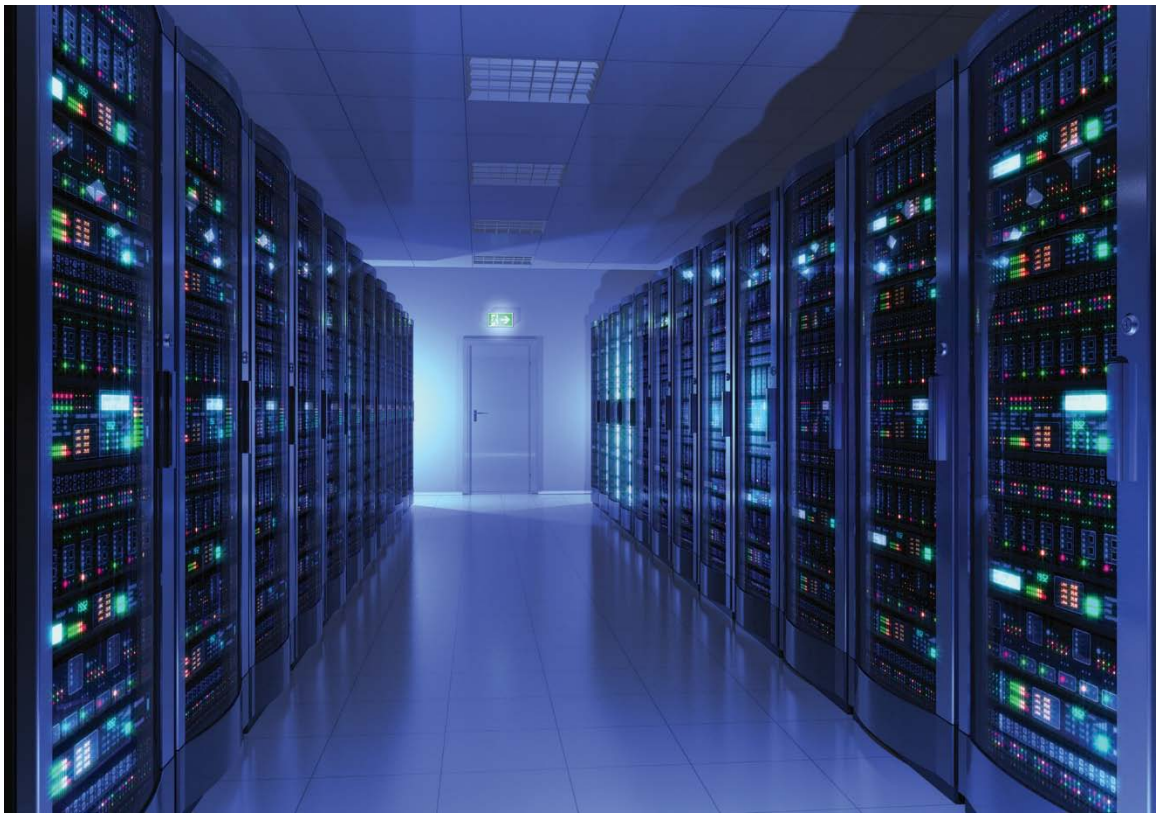
The Data Center Emulator focuses on enumerating the trends over the next decade that integrated electronics components and technology must meet for the Data Center Market. These trends particularly focus on:

- packaging technology and costs,

- PCB and connector technology and costs,
- testing and assembly/joining technologies.

INTRODUCTION

The DATA CENTER product emulator spans a portfolio of technologies that cover data centers and communications. Starting in 2013 the iNEMI roadmap[1] observed that networking and computing hardware was gaining more common components, as the communications becomes an integral part of enterprise computing and as technology advancements enable tighter integration of the communication and computing technologies in commercial business systems. This trend has accelerated in the 2015 iNEMI roadmap as the large data centers (known as the cloud data centers) have grown dramatically since the 2013 roadmap stressing the computing, networking and storage systems and the infrastructure on which they depend.



Traditional discrete server, storage and datacom applications have begun to merge in the data center and their OEMs have not necessarily kept pace with what large end users desire in the form of more integrated, 'open-source' data center systems. This merger has led to some industry turmoil and the emergence of end users as a more powerful factor in hardware selection. Companies like Google, Facebook, Apple and Amazon have begun developing their own 'erector-set' solutions to their data center needs.

[1] The Source for much of this material is the *High End Systems Product Sector* chapter of the iNEMI 2015 Roadmap

Data center products included by iNEMI and referenced by IHS include: mainframe and high-performance computers, the data centers and server farms that house the computers, communications equipment such as switches, routers and enterprise service provider equipment. An emerging topic in data center networks is disaggregation. Disaggregation refers to the dis-integration of the traditional server architecture to create modular, pooled resources—such as pooled microprocessors, pooled memory, or pooled storage. The interconnect technology both enables and limits this architecture, because the links that were previously contained on the server board must traverse an entire rack, multiple racks, or across data centers. Integrated photonics is an enabling technology for disaggregation.[2] Disaggregation promises improved efficiency and data capacity for the data center, but is limited by the cost and performance of the links. Latency requirements, in particular, impose hard limits on distances over which certain resources can be disaggregated. The question becomes: how far can the resources be relocated, and how much disaggregation can be cost‑effectively implemented? Latency requirements favor introducing solid state storage over disk storage even at a cost premium.

The trends identified in the 2013 iNEMI roadmap have accelerated in 2015. The number of devices connected to the data center has increased dramatically leading to a concept commonly called the IoT (Internet of Things). This second product emulator for the PSMC roadmap focuses on the integrated photonic needs and opportunities for billions of proposed IoT device adaptations, from appliances to HVAC, medical devices and factory automation.

The massive amounts of data from these fast growing elements are unstructured and the demand for analytics and fast movement of data is also accelerating. In addition, the importance of security has been repeatedly highlighted with multiple high profile situations gathering world-wide attention.

The Data Center of today is seeing a transformation from independent computing, storage and networking systems to integrated system units. This change is driven by the Internet of Things (IoT) that has quickly increased the number of devices that are interconnected and the increasing data center applications; thus, increasing the amount of data that is transmitted, sorted, analyzed and distributed. Figure 1 illustrates the growth in the number of interconnected devices, and Figure 2 illustrates the growth of data that is transmitted.

[2] Source: OSA Industry Development Associates (OIDA) *Roadmap Report: Photonics for Disaggregated Data Centers* (2015).

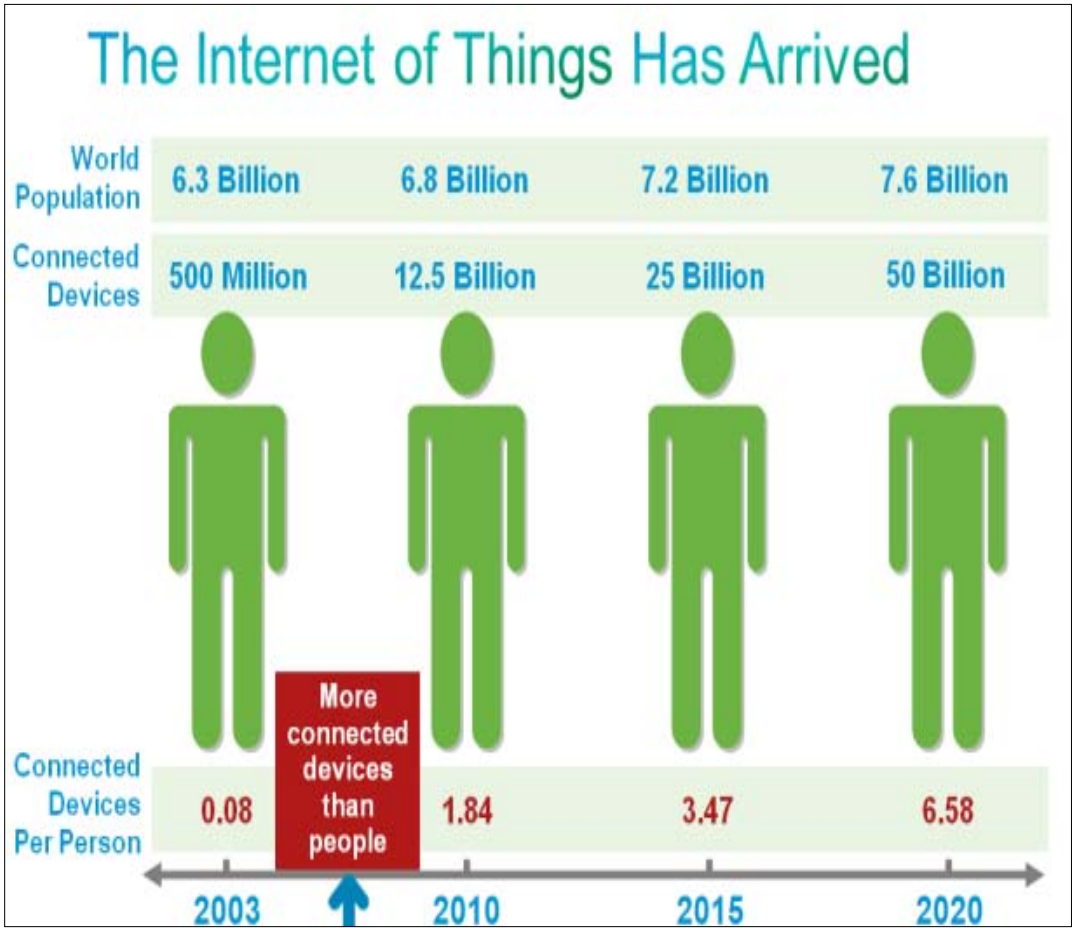


Figure 1: The Internet of Things was "born" sometime between 2008/9 and the number of interconnect devices is growing.

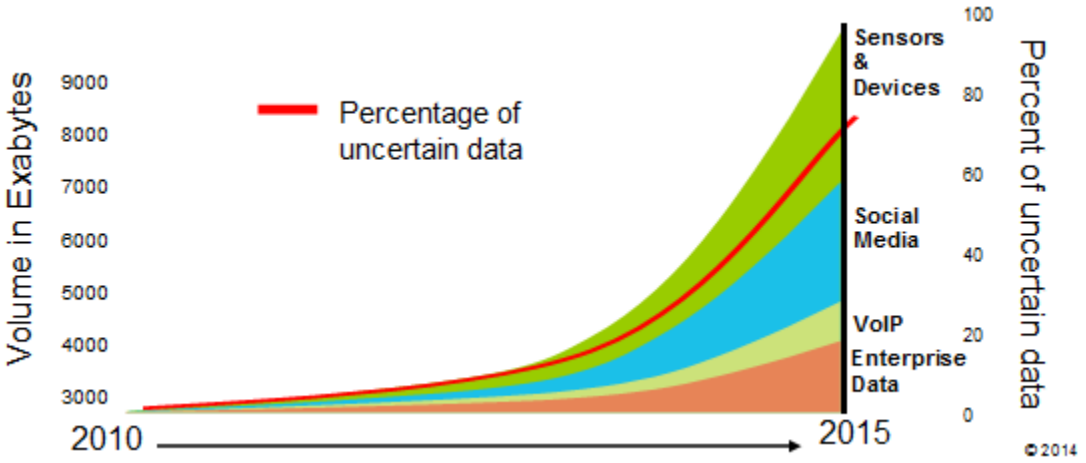


Figure 2: The amount of data that is produced is rapidly increasing.

The drivers of packaging requirements for Data Center includes the processor, storage, networking and switching fabric as interdependent subsystems that will continue to become more

integrated. The physical entities that constrain or direct development of packaging for these subsystems are the thermal, electrical, photonic and mechanical metrics that define the system characteristics.

These integrated electrical-photonic systems are aggregated in data centers that are the infrastructure that serves cloud computing. The cloud data centers make up the fastest growing segment of Data Center.

Thermal and power management of the system continue to be major challenges for Data Centers. A key component of the total cost of ownership is the cost of the energy to power the high-end equipment and, in some locations, the amount of energy that can be delivered to a data center is at the limits of what the utilities can deliver. Thus integrated silicon photonic systems must equal or better electronic systems in terms of cost, energy use, and performance if they are to achieve widespread utilization in the data centers.

To achieve reduced energy use ASHRAE is creating standards where the temperature and humidity can be higher than has been traditionally required for high-end equipment. In doing so, there is less energy required to cool the data center. Therefore, there is a need for better thermal technology within the systems themselves to maintain acceptable junction temperatures of the silicon circuits and also active power management of the components that make up a system to maximize the power-performance of the systems. Also, more efficient power conversion will continue to be developed including voltage regulation close to the loads (such as in microprocessors) that significantly cut the power distribution losses within the system.

However, the biggest challenge is moving the data with low latency. The bandwidth requirements have resulted in the off die data rates continuing to increase even as the processor clock frequencies have stagnated. This change has been enabled by low power transmitter and receiver designs with continually advancing sophistication in the equalization techniques. The total amount of power for these interfaces is constrained by the amount of energy available as stated above. Also, the amount of parallelization of interconnect is limited by the expectation that the price of the interconnection will also be approximately constant. This results in the current trend of quickly increasing data rates per physical channel.

Packaging technology must increase at a rapid rate to achieve the new performance requirements. As breakpoints are reached, lower loss laminates, smoother copper, higher bandwidth connectors are required. Development of these components in high-volume manufacturing with cost competitive materials and processes is ongoing.

Optical interconnect is becoming more widely used with VCSEL data rates reaching 25 Gb/s and silicon photonics becoming commercially viable. The need for increasing bandwidth to move the data as well as the growing size of data centers defining the distance the high bandwidth interconnect must travel is creating more need for optical communication. At this time 3 meters seems to be the breakpoint between Cu and Fiber. As data rates pass 40Gbps on-board-on-chip photonics will be required.

The above factors of energy limits, efficiency, latency, and the growth of data transmission place a challenge on the processing power needed to perform the data analytics. A trend is starting to be observed where instead of more general purpose cores per chip and more threads per core, perhaps it is more efficient to employ specialty cores to do specific tasks. The use of GPUs and FPGAs allow quick turn-around time to quickly adopt more compute and energy efficient algorithms while special cores are developed to address specific computational tasks. As the big data era matures and 10 and 7 nm silicon nodes are developed, the packaging components to interconnect these components will also evolve.

SITUATION ANALYSIS

The growth of Data Center is shown in Figure 3 with a CAGR of 4.4%. Table 1 breaks out the growth of the individual segments: HPC and Mainframe computing, Data Centers, Enterprise Communications and Service Provider Equipment. Note that the Data Centers are the fastest growing segment. Table 2 breaks out the 2013 revenue by geography.

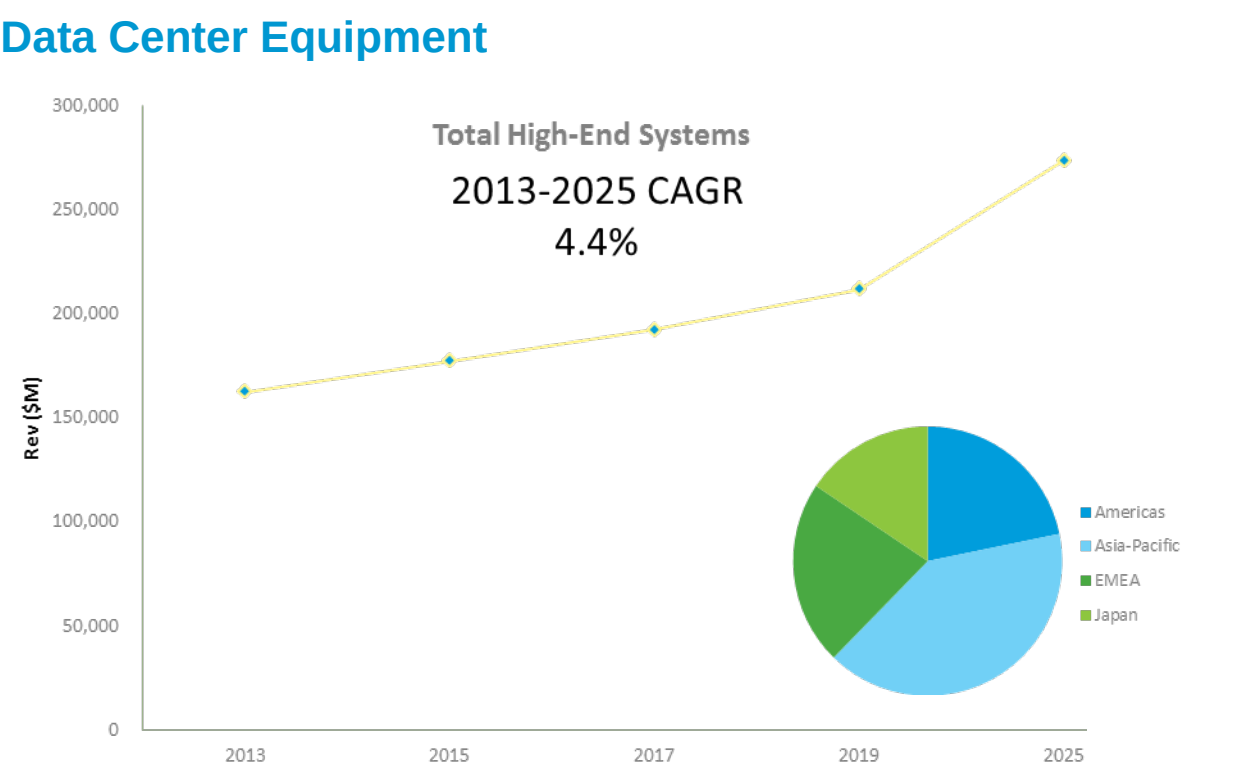


Figure 3: Data Center Equipment

DATA CENTER

Factory OEM Revenues ($M)

	2013	2015	2017	2019	2025	CAGR
Total Data Center	**162,280**	**176,972**	**192,202**	**211,776**	**273,436**	**4.4%**
HPC and Mainframes	24,036	24,207	28,146	33,340	42,874	
Data Centers	7,269	9,235	11,417	14,009	21,913	
Enterprise Communications	42,055	48,786	53,056	57,377	78,801	
Service Provider Equipment	88,920	94,745	99,582	107,050	129,848	

Table 1: Data Center OEM revenues

2013 Regional Revenue ($M)	Americas	Asia-Pacific	EMEA	Japan
Total Data Center	**35,317**	**65,801**	**35,888**	**25,274**
HPC and Mainframes	10,077	4,881	3,641	5,436
Data Centers	2,960	1,990	2,008	313
Enterprise Communications	6,460	24,928	4,299	6,368
Service Provider Equipment	15,821	34,002	25,940	13,157

Table 2: Data Center OEM revenues by geography

HPC AND MAINFRAMES

With regards to the High Performance Computing (HPC), Mainframe and Enterprise class server category, the need for big data analytics will continue to drive demand for these business critical servers. Although units of this mission critical server class account for only 12% of the total WW server units, revenue accounts for over 50%, given the high price tag for these systems. Growth remains fairly modest, and IHS estimates the high-end server unit and revenue CAGR over the 2012-2017 periods to hit 9.6% and 4.1%.

In the years to come, "Big Data" will still drive the need for these high performance systems. As these new classes of highly intelligent and computationally advanced systems begin to enter the market, the commercial benefits sector will become extremely valuable in making real-time data analysis available for quicker decisions and execution.

The need for the super-computers to continue to monitor and model the world's most complex data will likely not expire. However the high cost of these systems won't drive huge volume, but

they can be a technology driver, leading to more cost efficient means which can trickle down to other mainstream systems.

DATA CENTERS

The server market is undergoing an incredible acceleration of innovation, driven by the explosion of connected devices and the Internet of Things (IoT), resulting in disruption with changing requirements, workloads, and customization. The data center has become the largest server market driver for growth. In attempts to keep pace with the demand from the mobile and connected markets, IHS projects that servers going into the cloud will consume over 25% of total servers world-wide.

With the data center, a new breed of servers have entered the market - the density optimized servers or micro-servers - which are being created to meet the growing needs of the heterogeneous data centers and demand from connected devices. Innovations and technology of these new servers are being introduced at a rapid pace. Pure horse power is no longer the No.1 driver within the server industry. Power has moved to the forefront of demands. In the growing world of data centers and cloud build-out, servers must be efficient, use less power, and take up less space, all while meeting the specific workloads that the IoT requires. IHS projects that the micro-server will be nearly 20% of the total server market by 2019. This penetration may be mitigated by the lack of 64 bit ultra-low power CPUs, but the trend is there and too attractive to ignore.

However, despite the incredible demand coming to the data center, server unit demand will be somewhat tempered by the more efficient class of density optimized servers, as well as virtualization software, which can reduce server hardware resources 10:1. IHS is forecasting the revenue CAGR for servers going into the data center for the 2013, 2015, 2017, 2019, and 2025 period to reach 24%.

The new trend of “open sourcing” everything will drive innovation in this space faster than we’ve ever seen. With entire communities of engineers and resources working together to bring new products to market, it can be expected this market will proliferate, at least early on. However the security of the “Big” OEMs will still be highly valued, especially to smaller data centers that do not have the internal resources to manage everything on their own. These traditional OEMs will need to aggressively work and think outside their traditional means to keep up and maintain leadership, while providing life-cycle support in all aspects from hardware, to software, to support, to infrastructure.

SERVICE PROVIDER EQUIPMENT

The market for service provider communication equipment has been slow to recover from the global financial meltdown of 2008 and 2009 as normally conservative telecommunications operators became even more risk averse, halting almost all proactive equipment upgrades and deferring routine maintenance, and instead focusing spending to enable immediate revenue streams. The market started to thaw in 2013 as Telco’s resumed spending at near-normal levels. As the global economy continues its slow recovery, spending is expected to continue at this pace

for several years as Telco's resume normal maintenance and begin to upgrade core long-haul and metro networks.

Metro networks are already straining and must be upgraded, especially as the 4G LTE rollout becomes widespread. The capacity of long haul networks is in slightly better shape, but investment can't be put off and the 100 G Ethernet upgrade cycle has begun. Unlit long haul and metro fiber, in abundance since the late 1990s, is quickly disappearing, increasing the urgency for equipment upgrades. Existing communication applications and services are sufficient to fuel moderate growth in the mid-term.

While there is plenty of opportunity for growth in certain equipment types due to technology upgrades, the effect is somewhat offset by increasing levels of capex efficiency. As service providers increasingly move toward unified networks based on Internet Protocol (IP), they can reduce spending on supporting multiple types of legacy networks, such as the POTS (Plain Old Telephone Service) voice network. As multiple revenue-generating services migrate to a single flexible, high-capacity network, the ratio of capex to revenue will tend to decrease, notwithstanding the effect of short-term technology deployments.

While the short and mid-term market forecasts are driven by recovery and upgrades, the long-term health of the telecommunications equipment market is driven by the widespread adoption of new applications for communications technology. In this respect, there can be little doubt about the positive future for service provider equipment. The mobile internet is still in its early stages. The convenience of the ever-present connection has become a necessity, not a luxury, in every region of the world. Similarly, cloud computing promises to fuel long-term growth as cloud applications migrate value from the client to the network. Finally, we've only scratched the surface in our use of connected devices and the so-called "internet of things." Most households will evolve from a handful of internet connected devices to dozens and dozens over the next decade. Put together, all of these factors result in positive, but perhaps not extraordinary growth in the service provider equipment market through 2025. IHS expects the market to mirror or slightly trail global GDP growth during the period, about 3.2% compounded annually.

For integrated silicon photonic systems to grow at a rate faster than 3.2%, integrated silicon photonics must provide reduced system cost, increased throughput and a lower cost of ownership as compared to existing technology. The PSMC Technology Working Group (TWG) roadmaps quantify the requirements that must be achieved and the market opportunities that will be achieved.

ENTERPRISE COMMUNICATION EQUIPMENT

Compared to service providers, the enterprise market for communication equipment is more closely tied to short-term trends in the global economy, often anticipating economic trends a quarter or more in advance and reacting quickly. Therefore, the enterprise market has been in recovery since 2010, but cautiously, and ready to retreat at a moment's notice given the mere suggestion of a double-dip decline, sovereign debt default, or other economic setback. Today, most of these concerns have started to fade and the enterprise market is robust, in the sense that it is more capable of weathering minor setbacks.

Like the service provider equipment market, enterprise equipment spending is driven by technology upgrade cycles and a move to unified networks, two trends that are having a strong positive influence. However, enterprise spending is also driven by growth in employment, a component that has contributed little to enterprise spending over the past five years. New employees drive the need for more capacity in almost every part of the enterprise network, from additional LAN ports, to router capacity, to IP phones, and storage networking. IHS expects employment to mirror global GDP – slow but healthy growth over a number of years.

Enterprise networks are much closer to achieving unified networks than service providers. Nearly all enterprise data traffic is already IP data from end to end, with the exception of Storage Area Network (SAN) traffic. However, as Ethernet capacity grows to 10 gigabits per second and beyond in the enterprise space, even high performance SAN systems are migrating to Ethernet using protocols such as Fiber Channel over Ethernet (FCoE).

Technology upgrade cycles are also having a positive effect in the enterprise market. Around the world, IT managers are managing many new requirements for enterprise networks – compatibility with IPv6, 1 gigabit per second LAN drops, 10 gigabit per second switch backhaul, 802.11ac and subsequent Wi-Fi standards, traffic management, network security, and the "Bring Your Own Device" (BYOD) trend.

With technology upgrades as a constant upward pressure and the cumulative effect of slow growth in the global economy and employment, IHS expects spending in enterprise communication equipment to experience moderate growth through 2025, at a 5.4% compounded annual rate. Again, for integrated silicon photonic systems to grow at a rate faster than 5.4%, integrated silicon photonics must provide reduced system cost, increased throughput and a lower cost of ownership as compared to existing technology. The PSMC Technology Working Group (TWG) roadmaps quantify the requirements that must be achieved and the market opportunities that will be achieved.

ROADMAP OF QUANTIFIED KEY ATTRIBUTE NEEDS (2015 – 2025)

Following is a partial list of quantified key attributes extracted from the the High End Systems Product Sector chapter of the iNEMI 2015 Roadmap. In addition we have attempted to include specific key attributes unique to integrated photonics.

Table 3. Roadmap of Quantified Key Attribute Needs (2015 – 2025)

Parameter	Metric	2013	2015	2017	2019	2025
PCB Costs						
2 layer flexible	$ per cm2	0.03	0.025	0.025	0.02	0.019
4 layer flexible	$ per cm2	0.065	0.06	0.055	0.04	0.02
4 layer conventional	$ per cm2	0.012	0.011	0.01	0.008	0.006
6 layer conventional	$ per cm2	0.016	0.015	0.013	0.01	0.009
4 layer w/ microvia	$ per cm2	0.019	0.018	0.0165	0.013	0.01
6 layer, blind/buried	$ per cm2	0.032	0.033	0.026	0.02	0.01
8 layer	$ per cm2	0.03	0.0275	0.025	0.02	0.015
10 layer conventional	$ per cm2	0.048	0.045	0.042	0.035	0.02
10 layer w/ blind / buried	$ per cm2	0.095	0.09	0.08	0.06	0.03
14 layer, no blind/buried	$ per cm2	0.11	0.1	0.09	0.075	0.05
28 layer, blind & buried vias	$ per cm2	0.33	0.31	0.29	0.26	0.2
48 layer, blind & buried vias	$ per cm2	1.00	0.95	0.9	0.75	0.5
48 layer, (low loss material)	$ per cm2	1.30	1.56	1.79	1.97	NA
Assembly Costs						
Average Board Assembly Cost	¢ per I/O	0.75	0.7	0.65	0.55	0.35
Average Final Product Assembly Cost	$/unit	1300.00	1100	900	500	300
Package Costs						
IC Package Cost	¢ per I/O	0.18	0.16	0.15	0.15	0.12
Package Cost (High Density Ceramic/w/ Area Connector)	¢ per I/O	5	4	3	2	1
Package Cost (High Density µvia Laminate w/ Area Connecto	¢ per I/O	4	3	2	2	1
Connector Cost	¢ per I/O	1.90	1.6	1.3	1	0.5
Energy Cost	$/Wh	0.40	0.30	0.25	0.20	0.10
Memory Cost (Flash)	$/MB	0.18	0.15	0.13	0.10	0.05
Memory Cost (SRAM)	$/MB	0.18	0.15	0.13	0.10	0.05
Cost of Test as a ratio to assembly	ratio	0.40	0.50	0.60	0.60	0.80

Cycle Time						
NPI Cycle Time	Weeks	20	16	12	6	3
Product Production Life (not including spares)	Years	7	6	5	3	3
Reliability						
Temperature Range	Deg C - Deg C	"-40 to 85	"-40 to 85	"-40 to 85	"-40 to 85	"-40 to 85
Number of Cycles	Cycles to Pass	1000	1000	1000	1000	1000
Vibrational Environment (PWB level)	G^2/Hz	0.03	0.03	0.03	0.03	0.03
Use Shock Environment	Gs & ms to Pass	50G(2ms)	50G(2ms)	50G(2ms)	50G(2ms)	50G(2ms)
Humidity Range	% - %	UA	UA	UA	UA	UA
Altitude	Kilometers	NA	NA	NA	NA	NA
Force	Gs	UA	UA	UA	UA	UA
Devices						
Number of stacked die (Max)	#	3	4	6	6	9
Number of Die in SiP (max)	#	6	7	7	9	12
Passive Components						
Passive Devices:	Type/Size	0402 case	0402 case	0201 case	0201 case	01005 case
Embedded Passives	# per sq. cm	4-10	5-15	6-18	9-30	12-40
Max. Ohms	ohms / sq. cm	600	600	700	1M	10M
Max. Capacitance	µF / sq. cm	0.1	0.1	0.2	0.2	0.5
Min. % tolerance	%	10.00	5.00	5.00	1.00	0.10
Integrated Passives	nF / sq. µm	UA	UA	UA	UA	UA
RF Components						
Quality Factor	Q	125	400	1000	5000	7000
Capacitance density	nF/sq. cm	1	10	100	500	1000
Inductance req.	nH	30	300	1000	1000	10000
Interconnect Insertion loss maximum	db/cm/GHz	0.16	0.14	0.12	0.05	0.03
Memory						
Main Memory Type	Type	DDR	DDR2	DDR2	DDR4	DDR4
Main Memory Capacity	MB	2048	5196	10392	80000	1200000
Storage Type	Type	SATA/cFlash	SATA/cFlash	SATA/cFlash	SATA/cFlash	SATA/cFlash
Storage Capacity	MB	512-5196	1024-10392	2048-20784	50K	100K

Components/ Package						
Max Component I/O density	I/O/sq.cm	350	425	500	750	1000
Average Component I/O density	I/O/sq.cm	56	58	66	80	100
Average Component Density	#/sq.cm	2.4	2.8	2.8	3.0	3.6
Maximum I/O per package	I/O per part	5000	6000	8000	10000	20000
Average I/O per package	I/O per part	275	300	325	400	500
Max Components/sq. cm.	#/sq.cm	2.4	2.8	2.8	3.0	3.6
Max I/O for 50 mm square SCM w/ full area array	#	4096	4356	4900	7056	10000
Max I/O for 100 mm square MCM w/ full area array	#	10000	11025	12100	15129	20000
Package I/O Pitch, (area array)	mm	1.00	0.75	0.75	0.80	0.50
Package I/O Pitch for SCM (area array)	mm	1.00	0.75	0.75	0.80	0.50
Package I/O Pitch for MCM (area array)	mm	0.90	0.85	0.80	0.70	0.50
Package I/O Pitch (perimeter)	mm	0.40	0.35	0.30	0.25	0.20
Number of Terminals - Max Digital	#	1200	1350	1500	2000	2800
Number of Terminals - Max RF	#	475	550	650	1000	1500
Maximum Component Height	mm	NA	NA	NA	NA	NA
Maximum Body Size (L x W)	mm	50	60	80	100	150
Minimum Terminal Pitch BGA	mm	0.5	0.5	0.4	0.3	0.3
Minimum Terminal Pitch Leadless	mm	0.5	0.4	0.4	0.3	0.3
Minimum Component size (LxW)	mm	1.0 x .5	.6 x .3	.6 x .3	.5 x .25	0.4x.2
PCB / Substrates						
PCB Board Size (Min)	sq. cm	300	300	250	200	200
PCB Board Size (Max)	sq. cm	3000	3000	3000	3000	3000
Substrate Lines/Spaces	µm	25/25	20/20	10/10	6/8	3/4
Substrate Pad Diameter	µm	300	280	250	180	100
Ceramic Thin Film Lines/Space	µm	14/14	8/10	6/8	1/2	1/2
PCB Land Diameter With Vias for BGA - Via in Pad (VIP)	µm	500	450	400	300	250
PCB Backpanel Size – Area	sq. cm	3000	3000	3000	3000	3000
PCB Minimum Plated-thru-via (PTV)	mm	0.2	0.2	0.15	0.15	0.10
Substrate Material	Type	FR4	Low Loss	Low Loss	Super Low	Super Low
PCB Lines And Spaces	µm	75/100	75/75	75/75	63/75	50/60
Substrate uVia Diameter	µm	70	55	40	40	30

Interconnects						
I/C Pkg-to-Board	Package	PGA/uLGA/FCBG/	uLGA/FCBGA	uLGA/FCBGA	uLGA/FCBGA	uLGA/FCBGA
Discrete Wire	Type	IDC	IDC	IDC	IDC	IDC
Display -to-Board	Type	FEC	FEC	FEC	FEC	FEC
Pitch Width	mm	0.4	0.4	0.4	0.3	0.2
Memory	Type	MM/SO-DIMM/uBG	MM/SO-DIMM/uBG	SO-DIMM/uBGA	SO-DIMM/uBGA	SO-DIMM/uBGA
Printed Circuit	Type	Mini-PCI	Mini-PCI	BGA-Mez	BGA-Mez	BGA-Mez
IO	Type	USB3.0 / XFP	USB3.0 / SFP+	USB4.0 / SFP+	EO	EO
IC Card	Type	PC-SFF	PC-SFF	PC-SFF	PC-SFF	PC-SFF
Connector Minimum Mated Ht. (Board-Board)	mm	2.5	2.5	2.3	2.0	2.0
Compliant Press Fit Pins	mm	UA	UA	UA	UA	UA
Minimum Connector Pin Pitch	mm	1	1	0.8	0.5	0.3
Electrical & Test						
Frequency on Board	MHz	4000	6000	10K	15K	20K
Impedance Tolerance	%	7	7	5	5	3
Number of Voltages	#	10	10	12	12	14
Off Chip Driver Rise Time	V/ns	25	30	35	50	100
Serial Bus Rate (1 bit)	Gb/s	8	10	14	24	40
Built In Self Test (BIST)	%	50	70	85	90	95
Boundry Scan	%	20	35	50	75	85
Test pad access minimum	%	25	20	15	5	3
Maximum escape rates	DPMO	500	400	300	200	100
Power						
Power	Type	Li-Ion/AC	Li-Ion/AC	Fuel Cell/AC	Fuel Cell/AC	Fuel Cell/AC
Spec. energy	Wh/kg	175	200	300	400	700
Energy dens	Wh/liter	500	550	600	800	1000
Cycle life	#cycles-80%	500	600	1000	1500	2000
Specific power	W/kg	1500	2000	2500	4000	6000
Shelf life	years	3 years	4 years	5 years	8 years	10 years
Max. switching noise	% voltage	0.10	0.07	0.05	0.05	0.03
Avg. standby power	Watts	0.05	0.05	0.05	0.05	0.05
Min. and Max. Operating Temperature	Degrees C	0 / +65	0 / +70	0 / +70	0 / +70	0/+70

Environmental						
Minimum MSL Level	Level #	1 ~ 4	1 ~ 4	1 ~ 4	1 ~ 4	1 ~ 4
Max Reflow Temp	Degrees C	230	250	265	265	265
Solder Type	Composition	SnAgCu/SnPb	SnAgCu/?	SnAgCu/Pb Free	SnAgCu/Pb Free	SnAgCu/Pb Free
Recycling targets - Recovery, Recyclability	%,%	70/60	75/65	80/70	95/90	98/95
Thermal						
Use Ambient Operating Temperature Range	Deg C - Deg C	-10 to 50	-10 to 50	-10 to 50	-10 to 50	-10 to 50
Thermal Design Power (Hottest Chip)	Watts	225	225	225	225	225
Max Current per Device	Amps	250	280	280	280	280
Use Relative Humidity	% - %	85	85	85	85	85
Thermal Design Flux (Hottest Chip)	W/sq. cm	90	100	105	105	105
Cooling Method	assive,Active, None, Bo	Passive	Both	Both	Both	Both
Number of Chips W/Some Heat Sink	# / Assy or Board	6	6	8	16	26
Device Cooling Air Temperature (Inside the Box)	Deg C	50	50	50	50	50
Device Cooling Rail Temperature	Deg C	NA	NA	NA	NA	NA
Chips W/ Power < 2W	/ Per Assembly or Boa	400	400	300	200	100
Chips W/ Power From 2 - 5 W	/ Per Assembly or Boa	6	6	6	6	6
Chipc W/ Power From 5 - 10 W	/ Per Assembly or Boa	8	6	6	6	5
Chips W/ Power > 10 W	/ Per Assembly or Boa	5	5	4	3	2
Module Power	W / sq. cm.	UA	UA	UA	UA	UA
Acoustic Limitation (Air Flow/Fan)	db	UA	UA	UA	UA	UA

CRITICAL INFRASTRUCTURE ISSUES

IDENTIFY PARADIGM SHIFTS

In the 2013 iNEMI Roadmap, the move to cloud computing was well publicized and a key component of providing the computing and data services for the nearly always available connectedness to on-line computing capability for both personal and business reasons. As portable electronics is growing quickly, the networking and data center infrastructure must grow to meet the demand. This shift is happening around the globe creating demands on the network bandwidth and the availability of the cloud computing and data processing.

These trends are continuing and accelerating in some areas as expected. It is still true that the data center cost and power is being held essentially flat, as the capability must increase to meet the cloud computing demands. For a computer system, this translates into increasing cost pressure as the system capacity grows, driven by more processor cores per socket, and more data bandwidth to memory. The virtualization and networking integration into the computer system tends to reduce the number of physical devices in a subsystem allowing room for even higher levels of integration. The amount of data being consumed, however, means the number of devices interconnected is increasing rapidly.

PRIORITIZED TECHNOLOGY REQUIREMENTS AND TRENDS

The packaging technology development for Data Center is currently driven by a need to process the quickly increasing amounts of data (Big Data) in a heterogeneous distributed environment (the Cloud). The attributes of these systems are discussed in the following paragraphs.

BANDWIDTH

The interconnect bandwidth demand is growing quickly. The bandwidth increase to now has been primarily provided with rapidly increasing bit rates per channel and incrementally increasing channel density. In 2014, systems can be built in high-volume with PCIe Gen 3 at 8 GT/s (Giga Transitions per second), DDR3 up to 2133 MT/s, optical OE devices at 10 GT/s and standards such as Ethernet at 40 Gb. By 2017, the PCIe Gen4 will be available at 16 GT/s, DDR4 up to 3200 MT/s, optical devices at 25 GT/s and 100 Gb Ethernet will be available on Data Center. As we go to 2020 and 2025, the challenge of getting enough reach which means enough length of trace to interconnect two devices and overcoming the loss of the trace will create the need for various signaling technologies. Both NRZ (Binary non-return-to zero data) and PAM (Pulse Amplitude Modulation) signaling will be developed with the appropriate equalization and application. Optical communication will become more broadly used as the cost and power of electrical interfaces at 25 GT/s and above will make optical communication more attractive. Silicon photonics is expected to become available in a broader range of applications because of the advantages of cost with silicon processing and packaging opportunity to create density of interconnections.

POWER

The challenge of electrical power defines the limits of how components are integrated, that is, the number of cores on a processor chip, the density of interconnect with the trade-off of the

signaling options of speed and optical vs. electrical. The footprint and content of rack electronics are constrained, and the availability of power from the utilities is capped in many installations. Therefore, the amount of power each rack and component can consume is constrained. A processor socket is expected to have a constant power demand going forward with voltages incrementally dropping so currents can increase. Voltage regulation (VR) will keep moving closer to the processor load to improve efficiency, especially with providing the voltage the circuits need for time-varying functions. The VRs will handle the incrementally higher current. In addition, other functions in the compute node will need improved voltage regulation to manage the powers for each component. For example, memory power also needs to be capped and will benefit from finer voltage regulation. The increased integration of storage and networking into the compute node also needs to be done without increasing the compute node power demand. The power limitations will constrain the function that can be integrated into the node so the need to optimize the power usage of each component becomes even more important.

THERMAL

The thermal capability, that is, the ability to remove heat from components and also from the frames that make up the system is at the limit of existing capability. Because the cooling of the datacenter also uses a sizable amount of power, the temperatures in the data center are rising while the chip temperatures must be maintained at a constant limit from generation to generation to maintain reliability at acceptable levels. At the component level, lower thermal resistant interfaces will be developed with advanced technology. The introduction of silicon photonic components will present a new challenge to maintain optical alignment and stability in this environment.

ENVIRONMENT

As more large datacenters are established globally, there is a broader range of environmental conditions that are encountered. Corrosive environments are encountered more frequently and the electronics must be able to withstand those elements. To maintain the power used for air handling in the datacenter, higher temperatures and higher humidity is being allowed by new ASHRAE standards. As packaged components are subjected to more moisture, the loss of interconnections will be increased which must be factored into the designs or materials chosen to minimize the impact.

LATENCY

Reducing the latency in communications in data centers is a paradigm shift that drives the need for new architectures such as disaggregation and the need to change from disk storage to solid state storage to reduce latency.

TECHNOLOGY CHALLENGES

The new technologies that are becoming available must meet the challenges of the previous section – bandwidth, power, thermal and environmental. Key new processor packaging technologies are being developed with some fundamental changes in the rest of the electronics industry and will impact the technology that can be leveraged. Most recently, the office and desktop computing hardware could be used for memory DRAM development, CPU and MPU core development, signaling protocols, and cooling hardware. With the increase in mobile

electronics, a new set of technology becomes available but at a much different scale of size and bandwidth than needed for Data Center.

The packaging and component technology that will be developed and integrated into Data Center will be those that successfully developed with acceptable cost and risk of adoption. Thus, the packaging for integrated silicon photonic component must utilize as much common technology as possible from the technology developed during the next decade for conventional electronic packaging. The following seven paragraphs discuss six packaging technology challenges. The first five challenges address challenges for electronic packaging. The last three address challenges for integrated silicon photonic packaging.

TSV: Through Silicon Vias are enabling 2.5D silicon interposers and 3D chip stacking providing high-density interconnect, and therefore, high bandwidth capability between components. Also, glass interposers may be a factor for some applications with Through Glass Vias (TGV) providing advanced connectivity. Memory modules are already introduced and applications will expand. The introduction of TSV has lagged expectations due to yield and cost issues which need to be addressed.

Advanced Packaging -- SiP and PoP: System in Package and Package on Package technologies provide the capability of optimizing cost and function in a package. Integrating voltage regulation and silicon photonics with processor chips or bridge chips will be increasing. The mobile systems are where the current growth driver in this technology segment originates. However, the Data Center will adopt these advanced package technologies because the increased interconnect pins, more memory, and more cores when placed in close proximity enables high-bandwidth interconnect in the existing power envelope. These tradeoffs will make the appropriate technology aspects economically scalable from mobile to Data Center.

Electrical connectors for packages and cards: Electrical interconnection will continue to be the dominant interconnection for short reach communication < 3m. The developing signaling standards are in discussion to go beyond 50 Gb/s per channel. Electrical connectors for printed circuit board and cable communication delivering low insertion loss, flat impedance profiles and minimal crosstalk will maximize the reach of the copper interconnect at an acceptable bit error rate. The speed of adoption of the higher speeds will depend on the ability to equalize the channels in the existing power envelope while the channel cost-performance as measured in $/Gb/s is reduced over time. The cost-performance is strongly impacted by bandwidth density. Bandwidth density can be channels x Gb/s/channel per unit area for a package on a printed circuit board or channels x Gb/s/channel per unit length for card edge interconnection. The required ground pins that provide shielding of signals and a continuous return path will increase the effective number of pins per channel. So even in cases where the channels per unit area or channels per unit length are constant, the number of pins may increase to effectively shield the signals. Use of Photonics signaling reduces many of these concerns and will be particularly effective when single mode interconnects and cabling are employed. The degree to which embedded waveguides will be used depends on a number of factors, but can be alleviated via on-board fly-over interconnects that use currently-developed optical receptacles.

Low-loss dielectrics for packages and cards: Reduced dielectric loss materials are increasingly used for the high-speed electrical channels and the demand for those materials will increase as speeds above 50 Gb/s/channel are adopted. However, low-loss electrical channels also require attention to processing and design of all the elements of packages and printed circuit boards. The copper roughness, via stubs, antipad size and shape, and internal via and PTH design are all as important as the loss characteristics of the dielectric material. Coreless packages and thin laminates for improved via and PTH design will reduce discontinuities significantly for high-speed channels. The footprint design at the electrical connector will require special design to avoid becoming the bandwidth limiting factor in a package to board, backplane or cable interconnection. This footprint design includes:

- Via, or PTH diameter,
- length and stub,
- antipad size and shape
- routing escapes from the vias, or PTH, and land sizes.

Reference plane gaps, holes and interconnection to PTHs that create return path discontinuities are part of the channel design.

Efficient power distribution: To efficiently address these technology challenges, the power efficiency must also continue to improve. The channel shielding requirements demand a greater amount of layers and vias for the high-speed channel. Improving the power efficiency demands lower impedance power distribution for less loss through I^2R loss and less inductance for faster regulation. This creates a trend towards more metal and placing regulation closer to the loads competing with the short reach signaling and increased signal shielding. These trends also leverage the advanced packaging concepts of TSV and SiP and PoP described above and is part of the economic driver to adopt this technology.

Optical Interconnects: Optical interconnect will be used more broadly. First, transceivers and active optical cables (AOC) will be used for in-frame communication, potentially replacing copper interconnect in backplanes or cables when the cost, power and bandwidth tradeoffs justify the switch to optical. Integrating optical devices into packaging to reduce trace length and, thus, power demand for high bandwidth interfaces will demand advanced heterogeneous packaging and leverage the SiP and PoP technology components for increasing integration at the package level. Low cost single-mode optical connectors will be needed to support pluggable electro-optical modules.

Silicon Photonics: The desire for higher levels of integration of optics will favor the adoption of silicon photonics. The system level cost management, integration density, and power limit trade-offs must be carefully considered as development of silicon photonics is pursued. The technology selected must leverage the existing silicon technology and infrastructure where ever possible to reduce both risk and cost.

CONCLUSIONS

Data Center growth is driven by the rapidly increasing amount of data and the number of devices that are interconnected. This product sector is forecast to have revenues continuing to grow at a CAGR of 4.4%.

The technology for high-end computing is driven by the quickly increasing number of interconnected devices and the resultant growth of data bandwidth between those devices. Meeting the demands of increased data bandwidth, processing and storage must be done under the constraints of capped available power and the expectation of prices to the user decreasing over time. The attributes that are important are the data bandwidth, power efficiency, thermal management and environmental conditions in which the systems operate. Addressing these challenges will require:

- Advanced silicon integration using stacked silicon with through silicon vias,
- advanced packaging integration built on the System in Package and Package on Package technologies (already in production use in mobile computing),
- optical interconnection for increased reach of bandwidth into the data center,
- silicon photonics to enable integration of optics,
- high-bandwidth connectors,
- low-loss materials and design features to maximize the reach of electrical interconnect
- power regulation integration to improve efficiency.

The increased performance that these enabling technologies will provide must be provided below the cost of existing technology for their adoption by the industry.

REFERENCES AND ACKNOWLEDGEMENTS

1. The 2015 iNEMI Technology Roadmaps have been used as a primary source particularly the High End System Product Emulator.
2. The data for Market Forecasts and Situational Analysis has been provided by IHS Technology.

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PSMC OPTICAL TRANSCEIVER COST MODEL

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PSMC OPTICAL TRANSCEIVER COST MODEL

EXECUTIVE SUMMARY

We limit our analysis to only the packaging of the optical devices into a module. The costs of components are taken as inputs and are not calculated directly. Although we carry out sensitivities to understand the potential implication of various levels of component costs, the reader should view this analysis as incomplete. Although incomplete, this analysis serves to demonstrate the potential for details process-based cost analysis to critical photonics questions.

Preliminary results suggest that

- monolithic integration of the Datacom transceiver has the potential to significantly lower packaging cost for both high and low volume production;
- the key cost savings opportunity for integrating in the near term derives from avoiding the expense of assembling and packaging the interposer layer;
- Integration has significant cost advantages even if optical chip yields were to fall well below baseline modeled values.

INTRODUCTION

The goal of the PSMC roadmapping effort is to identify the opportunities, obstacles and potential solutions to realizing broad adoption of microphotonics in a range of applications. In doing so, the industry will have the opportunity to coordinate resources and overcome those obstacles more efficiently. With a technology which is rapidly evolving, it is clear that there will be many potential solutions which are proposed to realize the future photonics vision. Each of those potential solutions will not only need to be vetted to ensure that they will provide adequate performance (e.g., speed and size), but also for their potential economic ramifications. It will be important to target industry resources on the portfolio of solutions which promise both the best technical and economic performance.

To address the latter part of this challenge, the PSMC roadmap is in the process of developing a generalized cost modeling tool that can be applied to bound the cost implications of proposed solutions. The goal of such a tool can be simply stated: to quantify the cost implications of proposed process flows. Such information should allow the roadmapping teams to focus their resources more rapidly – earlier in the technology development process.

Currently, the PSMC cost modeling tool focuses on the costs of packaging and assembly. The goal is to eventually expand that scope to encompass all relevant production related costs.
This chapter delves into the motivation for creating such a tool and then describes the current state of the PSMC tool primarily through a case example of optical transceivers.

CURRENT MODELING FOCUS

AN OUTLINE OF PREVIOUS WORK AND DESCRIPTION OF CURRENT NEEDS

Prior to the current PSMC effort, there have been relatively few published (i.e. publicly available) cost analysis studies that focused on the manufacturing of integrated photonics.

In the earliest such study, Schuelke and Pande analyzed the manufacturing cost of an optoelectronic integrated circuit chips based on a cost model developed for millimeter and microwave integrated circuits.[1] Specifically, they examined the economics of integrated four core functions (detection, preamplification, amplification & filtering, and decision making) into a single GaAs chip. Their conclusion was that integrating only two of the four functions was economically preferred because of decreases in net yield as the circuit grows in size and complexity. Marz et al. established an analytical model to estimate the relative yields and the relative costs over time of integrated optical chips to a reference chip.[2] Their detailed model would allow decision makers to estimate how costs might be expected to change with integration and therefore optimize current levels of integration. As presented this model depends on the costs of an existing reference chip. As mentioned by the authors, to be complete, the scope of the model would need to be expanded to consider packaging and assembly of the complete module. An activity-based cost model is applied by Stirk et al. to calculate the cost of a 2-D VCSEL array communication module.[3] Although few details of the model are provided, this analysis makes clear that assembly yield is a critical aspect of ultimate module cost.

More recently, the research team at MIT built upon these various earlier studies. Specifically, Kirchain, Fuchs et al. from MIT Materials System Laboratory developed a process-based cost model (PBCM) with data collected from numerous firms across the optoelectronics supply chain covering front end, back end and packaging. This model allows for the user to specify the process flow, individual processing conditions, operational characteristics, and level of automation at each step.

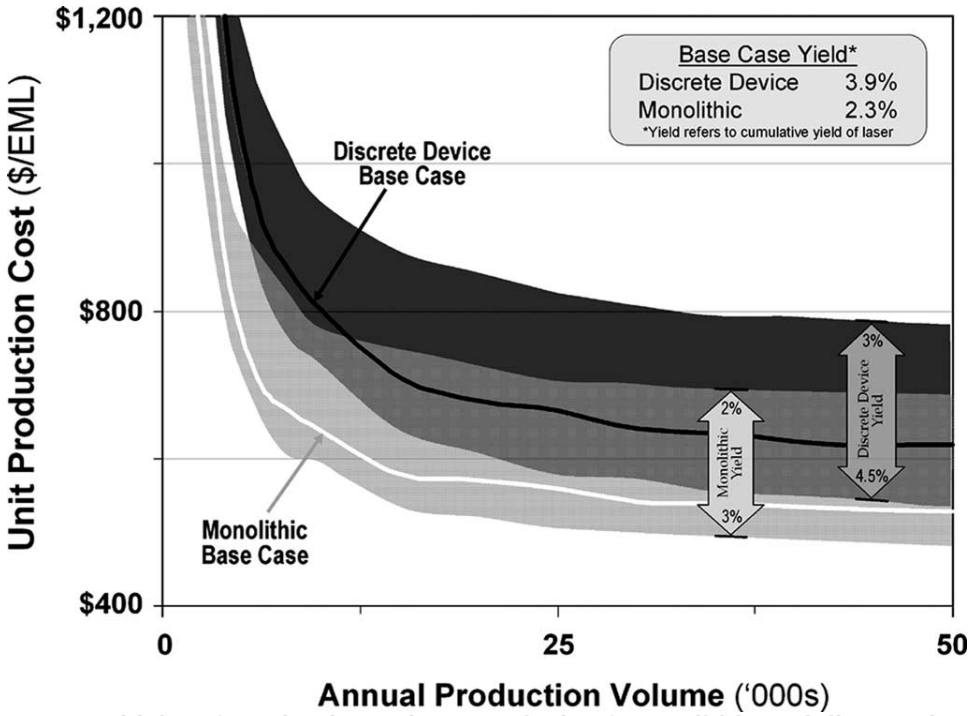


Figure 1. Cost sensitivity of production volume analysis of monolithic and discrete integration of InP-based DFB laser and EA modulator.

With the PBCM tool, the cost of integration of a 1550-nm DFB laser with an electroabsorptive (EA) modulator on an InP platform was analyzed.[4] The results suggest that a monolithically

integrated design should be more cost competitive over a discrete component options regardless of production scale (see Figure 1) unless the integrated yield is particularly poor. The research also identified the dominant cost drivers as packaging, testing, and assembly – the focus of current PSMC cost modeling activities. Besides, component alignment, bonding, and metal-organic chemical vapor deposition (MOCVD) are identified as processes where technical improvements were most critical to lowering costs. It is estimated that economies of scale for manufacturing the components occurred between 30,000 and 200,000 units/year, depending on the type and complexity of the device being evaluated, which encourages the photonic industry to consolidate its manufacturing sites in order to achieve economies of scale.

In a subsequent study[5], the optoelectronics PBCM model was applied to model transmitter designs with a Discrete Laser and Modulator (Prevailing Design) and an Integrated Laser and Modulator (Emerging Design) and study the impact of off-shore manufacturing on optoelectronics. It was found that the economics of offshore production increases the cost advantage of the prevailing technology and therefore reduces incentives for innovation (see Figure 2).

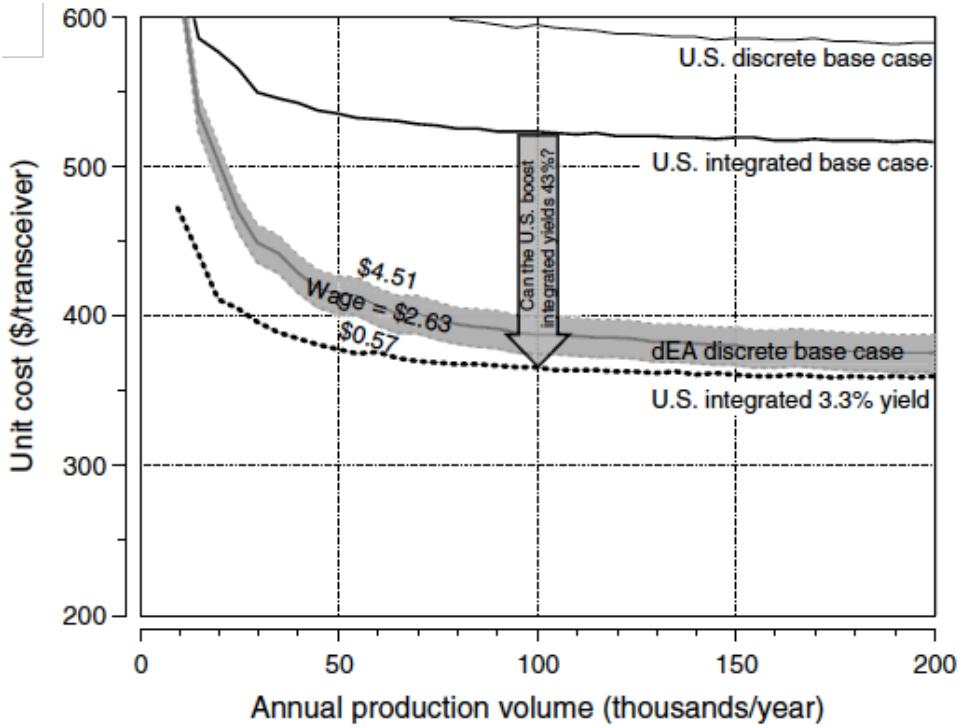


Figure 2. Cost competitiveness of U.S.-produced integrated laser modulator vs. developing East Asia (dEA)-produced discrete laser and modulator design.

Finally, in a third study[6], the MIT research team explored the competitiveness of two Si photonic designs against InP-based alternatives for a 1310 nm, 100 gigabit ethernet LAN transceiver. The research suggested great promise for silicon photonics to meet cost targets in midterm server and storage area network applications and to provide even lower cost devices for future, high-volume consumer and mobile computing applications. Specifically, it was found that silicon photonics holds great potential to be cost competitive in markets with annual sales volumes above 900 000,

including servers, computing, and mobile devices (see Figure 3). These results should motivate academic research into integration on the Si substrate from the perspective of cost.

These previous studies provide an important foundation on which current cost modeling efforts and tools can be built. Nonetheless, there are some important gaps which the PSMC effort is currently addressing. Previous studies primarily focus on optical transceivers for telecommunication applications. Currently, however, attention focused onto the application of optical transceivers in data centers. More pointedly, the application of transceivers for shorter distance applications inherently face stiffer cost challenges. Hence, for the current roadmap development, the model's target needs to be shifted.

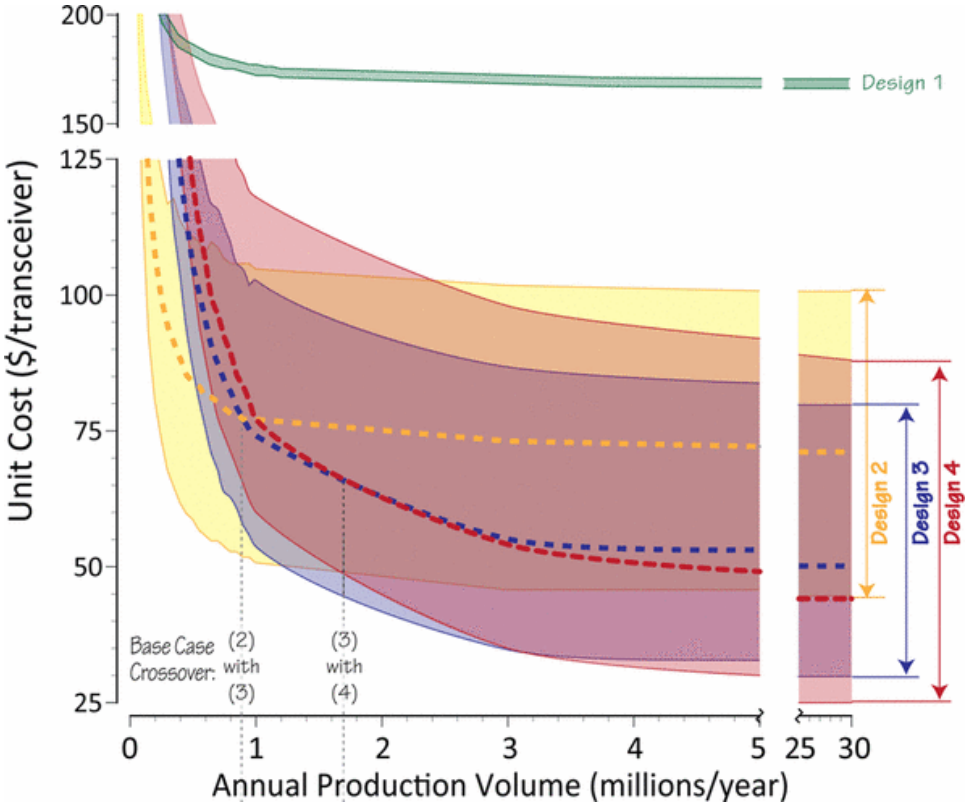


Figure 3. Total cost comparison of InP based designs (1: TOCAN and 2: DML) and Si based designs (3: Hybrid and 4: Silicon Two Chip) with yield and regional sensitivities (top and bottom bands plus base case yield bands).

This is particularly relevant because the packaging processes for data center optical transceivers differ from those used in telecommunication applications because the datacom optical transceivers are based on more compact designs. For instance, as mentioned in the Assembly & Test Chapter, for accurate assembly of small optical parts in datacenter optical transceivers (e.g. single mode optical fibers), alignment of parts to <0.1 micron of accuracy is demanded and there is a trade-off between speed and accuracy for a decision between passive alignment methods and active alignment methods. Furthermore, since these earlier studies were completed, more packaging technologies have emerged, such as high aspect ratio through silicon vias and thermocompression bonding. Last but not the least, the integrated photonics and electronics technologies are evolving quickly and thus the input data needs to be updated. Therefore, to

support the current photonics roadmap development activity, the cost modeling team has been updating the cost model to target data center-oriented transceiver designs, add in new packaging processes, and update the input data.

CURRENT MODEL OVERVIEW

The PSMC cost modeling tool is a process-based cost model (PBCM). As such, the tool builds up cost from technical details. These details are used to estimate processing requirements (e.g., time and materials) and thereby resource requirements (e.g., equipment and personnel). From resource requirements it is possible to project future cash flows and, therefore, compute various cost-related metrics.

The model focuses on packaging processes of emerging designs for integrated optical transceivers in data centers. Because of this focus on packaging, costs of components (laser, interposer, etc.) are directly taken in as inputs instead of being calculated starting from raw material. The final cost of an integrated optical transceiver module is determined from the cost incurred for each step of the manufacturing process. The total cost is the sum of step costs and unit cost is total cost divided by production volume. For each step, the cost is projected by first mapping physical parameters of product designs to production process requirements (e.g., material and thickness requirements to their implications for cycle times, downtimes, yields). These relationships are determined using physical models or through statistical methods. The model then maps these production process requirements to the quantity of production resources (e.g., kilograms of material, person hours, and number of machines) required to meet a stated production scale target. After that, the model multiplies these resource requirements by their respective prices to determine the step costs.

During calculating step cost, the cost is further broken down into primary categories: machine cost, tool cost, building cost, material cost, labor cost and energy cost. For machine cost, the model estimates the quantity of machines required to meet production goals based on available operating time each year and the required machine time to produce the product at the targeted production capacity. The number of required machines are multiplied with prices and annualized (using a selected discount rate and conventional financial assumptions) to obtain annual machine costs. The calculation of tool cost is similar to that of machine cost except that the tool quantity is also subject to tool lifetime. In terms of building cost, there are three different types of cleanroom included in the model: Class 100, Class 1000, Class 10000 and the cost depends on the quantity of machines required and cleanroom space required by each machine. The material cost includes the cost of components (e.g. lasers, IC chips etc.), direct materials (materials that are integrated into the product e.g. metal, bonding paste etc.) and indirect or process materials (water, carrying gas etc.). To estimate labor cost, the model considers personnel of different skill levels to accommodate both highly automatized processes (that require labor with less skill) and relatively complex processes (e.g. visual inspection, active optical alignment, etc.) that require specialized skills. For energy cost, the current model considers only the energy used to power machines; energy required to power the cleanroom facility is included in the building cost as part of the building maintenance cost. In future versions, energy costs will be modeled more explicitly such that it is a function of production volume, machine power and clean room facility working hours.

As a successor of the earlier version of the MIT Photonics PBCM, the current model retains flexibility for the user to define process organization (i.e. the order of the process flow), processing conditions, operational characteristics, and level of automation at each step. Meanwhile, an improved model structure considerably reduces the work for definition of new processes and thus new processes can be conveniently added in the model and it is expedient to compare different processes.

CASE ANALYSIS

To gain insights into the production economics associated with integrated photonics, we analyze the relative economic competitiveness of three functionally equivalent datacenter optical transceivers. While the economics of the optical transceiver case will be of interest to some readers, we expect the underlying production economics to hold true beyond the specifics of the case and designs chosen.

The three transceiver designs (see Figure 4) selected to are: 1) Hybrid: laser, fiber array and IC chips mounted on active optical interposer; 2) Monolithic with hybrid layer: laser and fiber array mounted on optical and electrical integrated chip; 3) Fully monolithic: fiber array mounted on optical and electrical integrated chip with laser integrated in the chip. Across the three designs, the level of integration increases.

The cost of producing the individual chips is not modeled explicitly. Instead, we assume that chip production costs are proportional to the area of the chip and estimate that area. Also, initially we assume that yields for all chips are the same. Clearly that will not be the case. As such, we explore the sensitivity of the result to changes in yield.

CRITICAL CAVEATS

- For all three designs, we limit our analysis to only the packaging of the optical devices into a module. The costs of components are taken as inputs and are not calculating directly. Although we carry out sensitivities to understand the potential implication of various levels of component costs. The reader should view this analysis as incomplete. Although incomplete, this analysis serves to demonstrate the potential for details process-based cost analysis to critical photonics questions.
- The following analysis is based on data collected from less than three firms. As such, it is not statistically significant.

DESIGNS ANALYZED

The three transceiver designs (see Figure 4) selected to are: 1) Hybrid: laser, fiber array and IC chips mounted on active optical interposer; 2) Monolithic with hybrid laser: laser and fiber array mounted on optical and electrical integrated chip; 3) Fully monolithic: fiber array mounted on optical and electrical integrated chip with laser integrated in the chip. Across the three designs, the level of integration increases. As a result, the complication level of assembly process is decreased from the design 1) to design 3). In 1) Hybrid design, Tx/Rx IC chips, ASIC (Application Specified Integrated Circuit) chips and lasers are bonded to an active photonic

interposer wafer by thermocompression first. Then the interposer wafer is thinned to expose embedded TSVs (Through-silicon Via) from back surface, followed by backside metallization/UBM and wafer bumping. Next, the interposer wafer is sawed into dies. The die is mounted on an organic substrate and then the organic substrate subassembly is mounted on a PCB (Printed Circuit Board). Fiber arrays are assembled on the interposer dies at last. In comparison, in 2) Monolithic with hybrid laser design, the IC chips are integrated into the active optical interposer which becomes an optical and electrical integrated circuit (OEIC). Hence, only the laser needs to be mounted on the OEIC die before assembly with an the organic substrate. Moreover, with IC function and optical components (except light source) integrated in a single chip, high-density vertical interconnection through chip, TSV array, is no longer needed. Therefore, TSV-related fabrication steps (e.g. wafer thinning, backside metallization, etc.) doesn't exist in design 2) process flow. In 3) Fully monolithic design, the assembly process starts directly with the mounting of an OEIC with integrated laser chip on organic substrate since all the IC function and the optical components are already integrated into the single chip.

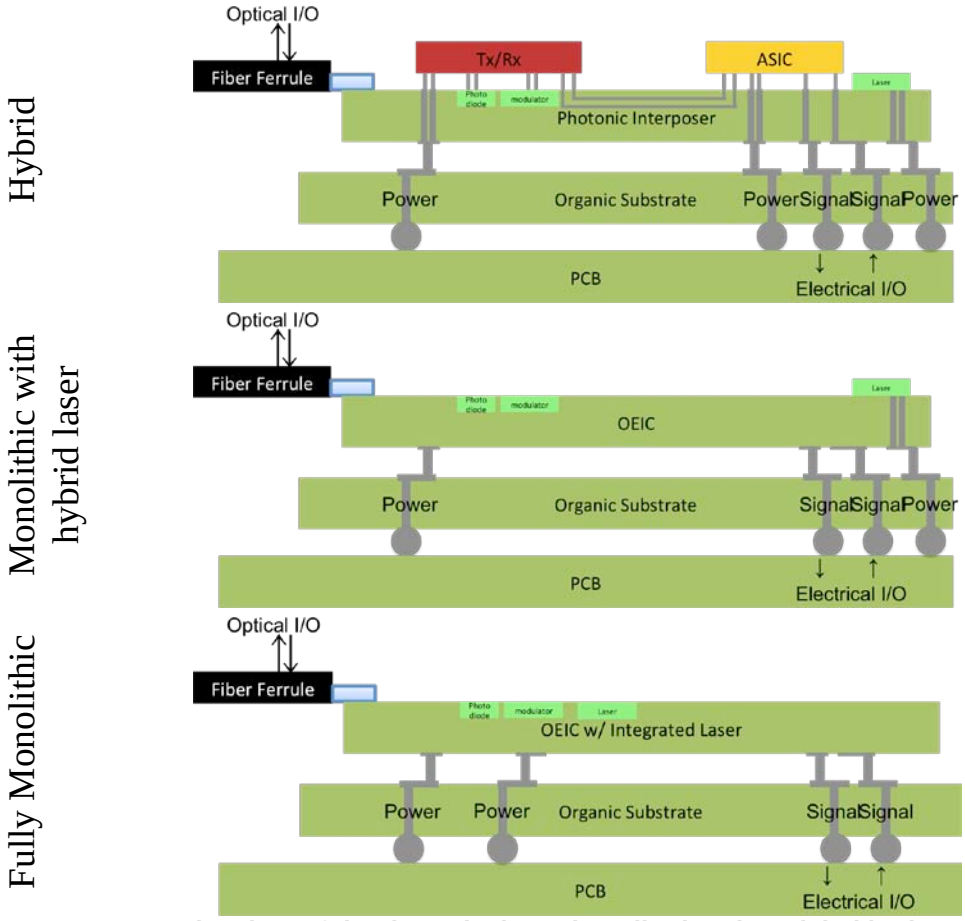


Figure 4. Cartoon sketches of the three designs described and modeled in the paper.

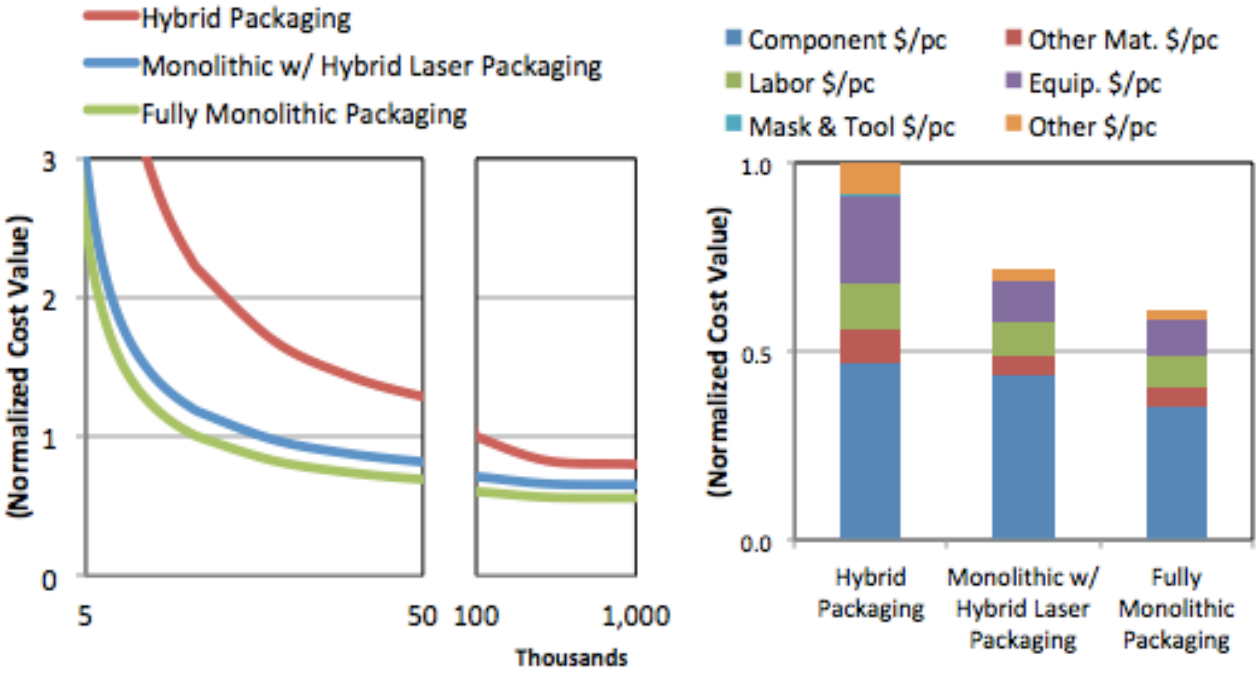
BASELINE RESULT

Figure 5 shows the modeled results for the baseline model conditions. These results suggest that the packaged cost of the integrated design should offer cost savings over various hybrid strategies.

A key advantage of the process-based cost modeling method is the ability to explore changes in both technological and operational conditions. One of the most cost-critical operational characteristic is production scale. Figure 5a shows that the model results predict that transceiver packaging costs are strongly a function of production volume. In fact, production volumes over 100k units per year appear to offer costs at least half of the costs at 10k units per year. Despite the fact that costs change significantly over thing range of production volume, the fundamental finding remains – these preliminary model results indicate a cost advantage for integration irrespective of production scale. Figure 5b makes clear that, at high volumes, the cost of the transceiver is ultimately bounded by the cost of the constituent components. For the fully integrated design, modeled results suggest that components would represent more than 60% of unit costs at 100k units per year. For the hybrid design, that cost is even higher, but only represents 45% of total unit cost.

Preliminary results suggest that monolithic integration of the Datacom transceiver has the potential to significantly lower packaging cost for both high and low volume production.

Although these results are preliminary, they suggest that integration offers real potential for reducing module cost. These results also raise two key questions: 1) What is driving the cost difference between the three strategies? and 2) How much do baseline conditions need to change before these results are changed?



a b

Figure 5. Baseline model result. a) Modeled unit cost versus production volume and b) Cost breakdown by cost element for the three different levels of integration

MAPPING THE DRIVERS OF COST DIFFERENCE

For roadmapping, it is important to not only quantify the expected cost difference between two alternatives, but also the drivers of those differences. As technology evolves, those drivers may be amplified or muted.

To explore this question, we apply the cost model in two different analyses. The first is summarized in Table 1 and Figure 6. These both present different perspectives on the cost differences among the three designs.

Table 1. Breakdown of modeled cost for the three designs at 100k units per year.

<table>
<tr><td colspan="2"></td><td colspan="2">Hybrid</td><td colspan="2">Monolithic w/ Hybrid Laser</td><td colspan="2">Fully Monolithic</td></tr>
<tr><td colspan="2"></td><td colspan="2">9 components,
17 process steps</td><td colspan="2">5 components,
8 process steps</td><td colspan="2">4 components,
7 process steps</td></tr>
<tr><td rowspan="4">Component</td><td>PCB / Org Sub / Fiber Array</td><td colspan="6">1 ea – 0.01</td></tr>
<tr><td>Optical Power</td><td colspan="4">1 – 0.01</td><td rowspan="2">1 Integrated die</td><td rowspan="2">0.29</td></tr>
<tr><td>Photonics</td><td>1</td><td>0.29</td><td rowspan="2">1 Integrated die</td><td rowspan="2">0.29</td></tr>
<tr><td>Circuits</td><td>4</td><td>0.04</td></tr>
<tr><td rowspan="3">Process Step</td><td>Optical Component Assembly Steps</td><td colspan="4">2 – 0.09</td><td>1</td><td>0.07</td></tr>
<tr><td>Other Assembly Steps</td><td>12</td><td>0.33</td><td colspan="4">3 – 0.07</td></tr>
<tr><td>Test Steps</td><td colspan="6">3 – 0.05</td></tr>
</table>

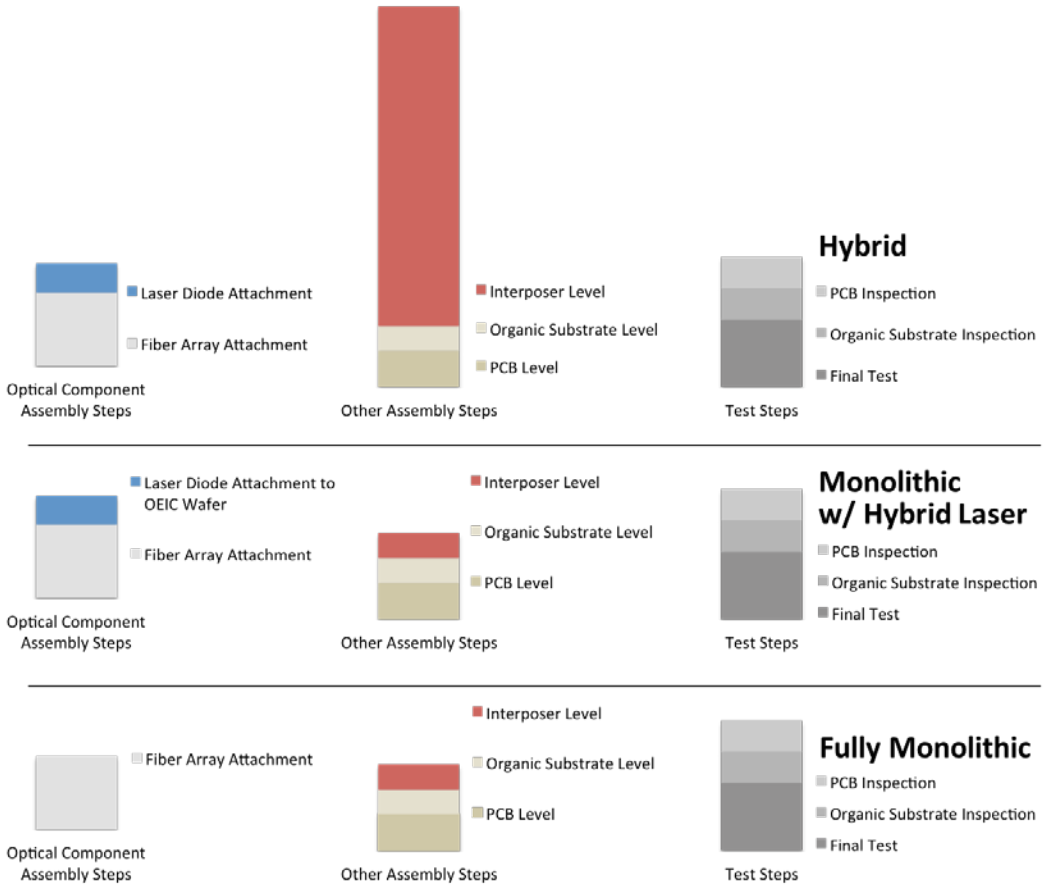


Figure 6. Breakdown of modeled costs by activity. To highlight differences, the activities are grouped by those related to i) optical component assembly, ii) other component assembly, and iii) test steps.

This analysis suggests that the largest drivers of cost difference across the three designs derives from a) the laser diode attachment (required for both hybrid designs) and b) the assembly of the interposer for the first hybrid design. As detailed in the table, the costs associated with the interposer are primarily from processing rather than components.

Preliminary model results suggest that the key cost savings opportunity for integrating in the near term derives from avoiding the expense of assembling and packaging the interposer layer.

As mentioned earlier, this current analysis very preliminary particularly regarding the cost assumptions around the optical chips. In particular, we assume that the cost of chips is constant per area and that the yield is similar for each chip. To understand the implications of these simplifications, we explored how the cost would vary depending on the yield of the chip. In particular, we quantified the total module cost at a range of chip yields for each of the three designs. Using this information we identified the point at which a lower yield for the two more integrated designs would climb to parity with the more conventional hybrid design. This analysis is plotted for a production volume of 100k units per year in Figure 7. From this, we can see that that model suggests that the cost advantage of the Monolithic with Hybrid Laser packaging would remain cost competitive even if yields fell to 60% and the Fully Monolithic packaging would remain competitive at yields well below 50%.

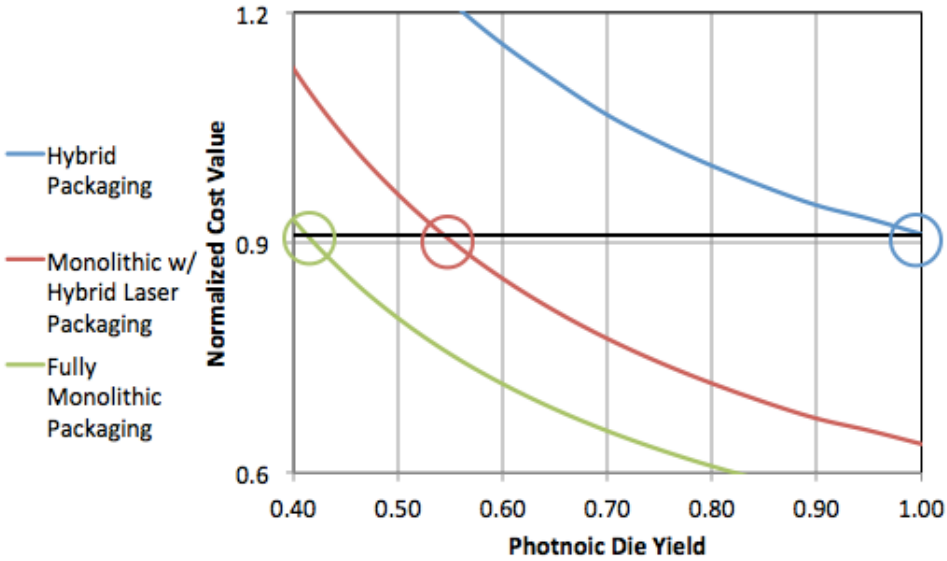


Figure 7. Yield sensitivity of three designs when annual production volume equals 100k units per year. Black line indicates packaging cost of the Hybrid design for baseline yield conditions.

Preliminary model results suggest that integration has significant cost advantages even if optical chip yields were to fall well below baseline modeled values.

CONCLUSIONS

The model results presented here are very preliminary and should not be interpreted as providing specific guidance. Nevertheless, the analysis presented in this chapter indicate the potential for such tools within the roadmapping process. In particular, these tools will allow the TWGs to

isolate key points of cost leverage and to explore the cost ramification of promising technical solutions.

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MONOLITHIC INTEGRATION TWG

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MONOLITHIC INTEGRATION TWG CHARTER

The Monolithic Integration Technical Working Group was commissioned with the following charter.

- Evaluate the imperative for future technologies to employ highly integrated photonic systems.
- Catalog the Technology Roadmap for Integrated Photonics Technology.
- Identify Roadblocks and potential Show-Stoppers holding back these developments.
- Communicate this information to the industry supply chain, the AIM program and its stakeholders.
- Continue to catalog this evolving technology roadmap as more is known about the strategic imperative for integrated silicon photonics technology & manufacturing in the US.

This TWG assesses the manufacturing ecosystem for i) chip-level integration on the Si and InP platforms, ii) design for manufacturing, iii) trade-offs among cost, energy, bandwidth density, and functional latency.

The 25 year view will include roadmaps for functional optical components: optical engines, switches, sensors, and processors. Fulfillment of the charter has incorporated discussions and research among more than 50 TWG participants.

EXECUTIVE SUMMARY

The advent of cloud computing, supercomputers and short data center product cycles have created additional demand for board and I/O-level photonic components and subsystems, including rack-to-rack interconnects in data center applications, 40-100 Gbps Ethernet and numerous specialty applications where RFI and other environmental issues favor optical interconnection. A current rule of thumb for data centers is Cu < 3 meters and fiber beyond. For high performance computation (HPC) systems, the rule is photonic interconnection > 0.05 meters. This E-O technology transition will move inward as data rates exceed 100Gbps/channel, or where the compelling advantages of photonics: lightweight, less power consumption, lower cost per bit, are determining. On-chip Al and Cu wires are constrained on the short side by power density and on the long side by latency and loss. The only viable solution is increasing use of photonic circuitry near the CPU/ASIC and outward, ideally with seamless on-chip/off-chip photonics, rather than converting signals from electrons to photons *outside* the package. Photonic interconnection is currently being accomplished with a range of multichip solutions, including Si, GaAs and InP devices in various transceiver modules and active cable assemblies.

Aggregate interconnection data rates of Tb/s and Pb/s will be required (1,000 – 10,000 Gb/s) within this decade. This transition to photonics will still require parallel system buses, aiming toward 100Gb/s/channel. These interconnects will be needed in larger, increasingly complex data center, router, switch, computer server-storage equipment and scientific computer applications. Integrated photonic technology, will be required to scale system performance without enduring massively parallel Cu circuits and their attendant high power budgets and increasing system costs. Great strides have been made in adopting Si electronic device technology to photonic lasers and detectors. Commercial introduction of these developments has been limited to a handful of major Si IC manufacturers. A number of datacom system players, E-O transceiver, and value-added connector manufacturers are providing what might be classified as interim solutions in this area. Universal industry goals are i) to achieve acceptably low power budgets; ii) to provide photonic signaling in the Tb/s range, and iii) to use lower cost Si/CMOS capabilities, including existing processes where possible, to reduce the cost of photonic systems to the silicon IC paradigm.

The Integrated Photonic Systems Roadmap is a dynamic process, evident by the evolution of industry-wide semiconductor roadmaps over many years. The ITRS has reflected the semiconductor industry migration path from *geometrical scaling* to *equivalent scaling*. *Geometrical scaling* (e.g., Moore's Law) has guided targets for the previous 35 years, and will continue in many aspects of chip manufacture. *Equivalent scaling* targets improving performance through innovative system-level design, process, and software solutions that will increasingly guide the semiconductor industry in the future. Function-driven design requires incorporation of intelligent elements in the form of microprocessors, memory, and programmable logic devices built in silicon-based CMOS technologies. The *downscaling* of minimum dimensions enables the integration of an increasing number of transistors on a single chip, as described by Moore's Law. However, many quantitative requirements, such as power consumption and communication bandwidth no longer scale with Moore's Law.

Integrated Silicon Photonics research, development and commercialization initiatives address new functionalities that do not necessarily scale according to "Moore's Law".

- SiPh packages containing Si detectors, GaAs and InP lasers in SiP or PoP multi-chip designs.
- Fully integrated ICs that may in the future contain CPU/ASIC and Si photonic transceivers.

The so-called More-than-Moore approach typically allows for these functionalities to migrate from board-level modular applications, such as discrete transceiver packages and board-level interconnects, into a package-level (SiP), chip-level (SoC), Stacked Chip SoC (SCS) or Package-on-Package (PoP) solutions. What will a fully integrated Si-Photonic subsystem look like; and what are its design objectives? Table 1 depicts a likely path for this technology transition: discrete devices, to hybrid package assemblies, to integrated die functionality, to integrated photonic system-on-chip. Table 2 shows the projected integrated silicon photonics component deployment timeline.

Table 1. Silicon Photonics Technology Deployment

2015-16	2017-20	2020-25	Beyond
Discrete Devices	Interposers	EO CPU/ASIC	Logic-Memory-IO Integrated SiPh SoC Photonic Systems
EO Transceivers	InP VCSEL	Si Lasers	
Interconnect Modules	EO SiP/PoP	Multi-Die SiP	
MM Connectors	Fly-Over Cables	EO/Waveguide PCB	Wafer-Panel Substrates
MM Cables	MM-SM Connectors	SM Connectors	IO Connectors
AOCs	MM-SM AOC	SM Cables	Future WG

Interconnects Packaging SiPh Integration

Table 2. Silicon Photonics Components and Applications

Technology	Status
2015-16	
GaAs Lasers	VCSEL arrays commercially deployed in datacom
InP Lasers	Edge emitter arrays commercially deployed in telecom
Ge-on-Si Lasers	Research demonstration by several labs
Ge-on-Si Detectors	Fully waveguide integrated, commercially deployed
Waveguides	Si, SiON, SiN commercially deployed
SiP/SoC Assembly Technology	Electronics, but not photonics
Si Photonic Integration	Commercially deployed in cable and board assemblies
2017-20 Projected	
Ge-on-Si Lasers	Early market entry
Ge-on-Si Detectors	Pervasive commercial deployment
Waveguides	Pervasive commercial deployment, single channel
SiP/SoC Assembly Technology	Early 2.5 D deployment
Si Photonic Integration	Pervasive commercial deployment: cables and boards
2020-25	
Waveguides	Pervasive commercial deployment: WDM
SiP/SoC Assembly Technology	Pervasive commercial deployment: cables and boards
Si Photonic Integration	Emerging chip-to-chip intra-package
Beyond	
SoC Assembly Technology	Embedded in distributed circuit/system architectures
Si Photonic Integration	Transceiver-less: embedded electronic-photonic synergy

INTRODUCTION

The Information Age has introduced connectivity, control and analysis into most aspects of human existence. The pervasive deployment of new information applications has been enabled for the past three decades by the realization of short product cycle times with advanced manufacturing methods. The Grand Challenge for the next two decades is the continued exponential scaling of functional performance at a rate of 1000x every 10 years within essentially constant cost, energy and space envelopes.

Coordinated advances in hardware, software and system architecture are required. The end of transistor scaling requires parallel architectures to preserve energy efficiency. Distributed architectures require switches to scale the number of processing nodes, N, with linear rather than N^2 dependence. Global control and self-aware optimization rise to critical importance as system complexity and interconnection reach hitherto unanticipated levels. Special purpose components and systems, designed-for-function within the envelope constraints, will proliferate. Photonic functionality will migrate from communication to repartitioned communication and processing roles. Today's essential components, such as the optical transceiver, will dissolve into embedded roles in seamless photonic-electronic circuits and systems.

Each of the above trends relies on establishing an effective platform for component integration at all levels of the interconnection hierarchy. Monolithic integration is the desired end point for the currently perceived chip and module solutions. A monolithic platform eliminates interfaces that introduce cost, power dissipation and latency. A monolithic platform enables scaling by known design utility, and it facilitates faster time to market for manufactured products. A monolithic platform delivers manufacturing yield, throughput and tool utilization by solving manufacturing problems at a platform level. A monolithic platform enables tradeoff analyses among cost, energy and density.

Global trends in system architecture are driving changes that percolate to the chip level. Telecommunication networks, free from copper constrained bandwidth, are migrating back from packet switched to transparent, low overhead circuit switched architectures. Data center architecture is following the same path. HPC systems and multicore processor chips are adopting similar network configurations. Network dis-aggregation further drives a platform-based (permanently installed single mode fiber) interconnection infrastructure that facilitates optimization and retrofitting of function (processing, storage, switching).

The fundamental limitation for monolithic integration manufacturing is production volume. Monolithic integration delivers reductions in capital equipment, package, test and design cost and increases in overall production yield that scale with unit count. Pre-production development costs increase at a sub-linear rate with volume as chip complexity increases. Cumulative production drives the cost reduction learning curve. High production volume enables amortization of R&D, tools and personnel across multiple revenue streams, and it raises the threshold for investment in scaling through shorter product life cycles. If these thresholds are not met, hybrid assembly can effectively compensate for its lower yield and higher bill-of-materials with lower infrastructure overhead. Increasing system-level bandwidth requirements; parallel, distributed and dis-aggregated architectures; and shorter, scaling-driven product life cycles are driving monolithically integrated, electronic-photonic chip-level functionality. The rate of adoption is primarily limited by cost and by bridging the technology transition to electronic-photonic design. The optimum conditions for insertion of monolithic technology are i)

coincident growth of production volume with increasing design complexity to meet increased design cost, and ii) product volumes greater than one million units for a given supplier to amortize infrastructure cost.

SITUATION ANALYSIS: TRANSCEIVERS

The optoelectronic transceiver is the transducer between electronic signals used primarily for processing and optical signals used primarily for communication. Performance is measured in terms of i) cost, $ per Gb/s; ii) energy, pJ/bit; and iii) bandwidth density, Gb/s per cm^3. The primary differentiators in performance are data rate and transmission mode. Multimode (MM) platforms offer lower cost packaging and the energy efficiency of direct modulation. The one channel per fiber capacity limits bandwidth density. Bandwidth density is determined by chip-level laser array and vertically attached fiber bundle density. Single mode (SM) platforms offer greater reach and higher data rates with enhanced spectral efficiency through quadrature amplitude modulation (QAM) and wavelength division multiplexing (WDM). High bandwidth density is achieved with on-chip optical phase and wavelength channel multiplexing.

Key Points

- The transceiver is the near term driver for integrated microphotonics.
- Silicon is the only material platform capable of supporting a standard cross-market, high-volume transceiver in the long term.
- Initial optical cabling applications will be multimode; but board, module and chip level interconnection will be single mode.
- A WDM standard of ~20Gb/s per channel will optimize the tradeoff between power efficiency and aggregate bandwidth density.
- An *independent* optical power supply will be the dominant architecture in the near term.
- Optical pins will be needed within the next decade to address EMI and pin count issues.
- Multimode and short wavelengths (800-900nm) will dominate optical interconnects through 2018.
- WDM will be necessary to meet off-chip bandwidth needs by 2020: single-mode, long wavelength (1300-1600 nm) will be the standard.
- For large volume commercial applications**, transceiver chips** will stand alone from signal processing chips through 2020; and they will become monolithically integrated thereafter for chip-to-chip interconnection.
- The integrated silicon transceiver cost point in 2020 will be <$0.01/Gb/s (excluding laser).

Figure 1: Ethernet data rate and switch bandwidth saturation: front panel bandwidth is saturating at about 5 Tb/s. (compliments of Nicholas Ilyadis, Broadcom)

Board Level Optical Interconnects Figure 1 illustrates the faceplate bandwidth roadblock that is driving board-level interconnection architecture. Early implementations of 100GbE with pluggable form factors (CFP) has resulted in *reduced* front panel bandwidth. The solutions to this roadblock are following two paths: i) smaller circuit boards with new microserver form factors, and ii) optical transport on the circuit board.

Figure 2 gives the projected path to the end of the pluggable module and ultimate monolithic integration of the switch chip with a silicon photonic transceiver. The architectural strategy is to bring photonic transport closer to the signal source. Transport with copper traces can require two retiming operations to reach the board edge. Architectures based on transceiver-in-package or transceiver-in-interposer do not require retiming. Monolithic electronic-photonic integration with seamless photonic interfaces for transport optimize cost, energy and bandwidth density.

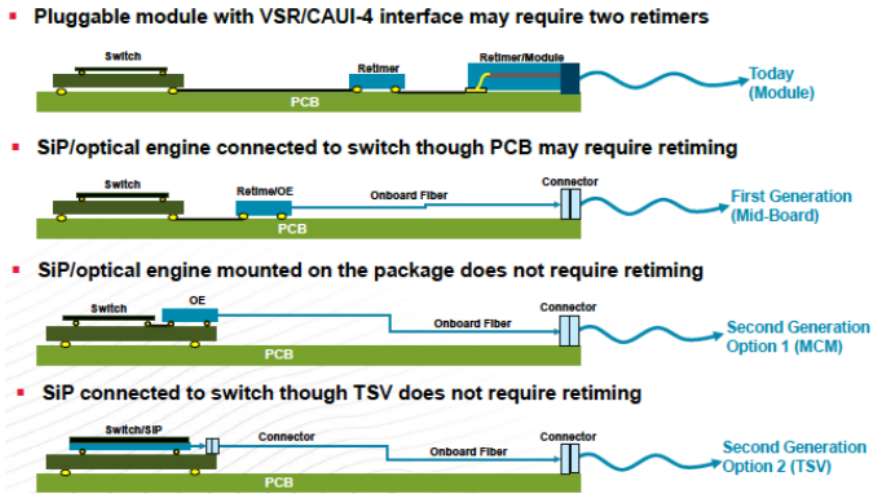

Figure 2. Sequence of line card implementations for increased bandwidth. (compliments of Nicholas Ilyadis, Broadcom)

The data center is the driver for high volume manufacturing of transceivers. Energy has become the disruptive agent for photonic manufacturing. Scaling of data center capacity at constant energy and space requirements has shrunk the 20 year telecommunication network rebuild cycle to 3 years for data centers. This new obsolescence factor has driven the technology transition to integrated photonics, and it has required significant research and development investment from the communication, computation and imaging product sectors.

Open Standards

The integrated photonics technology transition differs from the earlier integrated circuit transition, because there are no vertically integrated firms to envision and implement the system level tradeoffs among hardware, software and architecture in a way that preserves a standard platform and builds a learning curve for performance scaling at constant cost. As a result, de-facto consortia have arisen to organize the manufacturing supply chain for synchronous delivery of the components of a standard, scalable platform. These organizations recognize i) the fragmented, low volume nature of the current photonics industry, and ii) the growing use of optics in data center, consumer and industrial applications. They seek to create industry standards for interoperability, interchangeability and cross-market applications. Examples of these consortia in the data center area are the Open Compute Project http://www.opencompute.org and the Consortium for On-Board Optics (COBO) http://cobo.azurewebsites.net.

Disaggregation

The shortened data center product cycle time is requiring faster amortization of the hardware investment and, hence, higher incremental cost. To minimize long term investment, a permanent infrastructure with retrofit upgrades of modular compute, network and storage subsystems would be desirable. This architecture promises benefits of i) independent optimization of each modular component, ii) commoditization of identical modules with high volume manufacturing, and iii) commoditization of the data center system in much the same way as the personal computer (PC). Figure 3 shows a rack-scale server architecture proposed by in the Open Compute Project by Intel and Facebook. This architecture is adopting SM silicon photonic in place of MM VCSEL-based transceivers because i) any additional cost can be amortized over multiple product cycles and ii) SM is considered to be ‘future proof’ because of its compatibility with bandwidth density scaling through QAM and WDM.

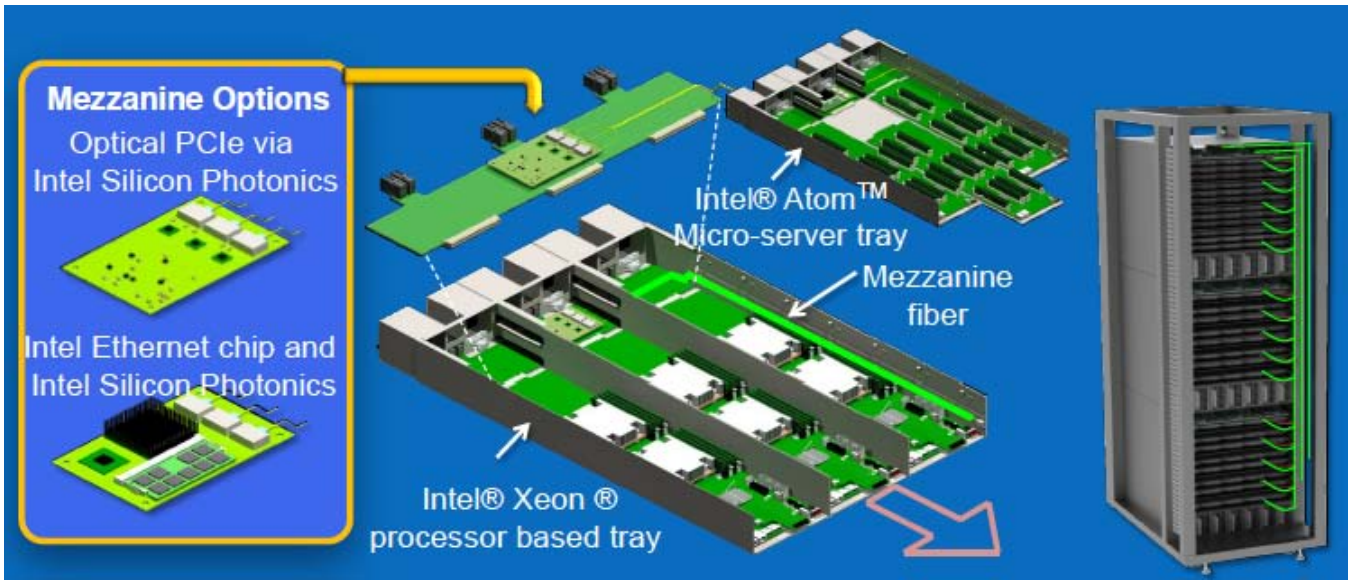

Figure 3. Disaggregated rack architecture based on a permanent SMF network infrastructure and board/backplane integrated silicon photonic interconnection. (Courtesy of Justin Rattner, Intel)

Software Defined Networks

Data flows are not uniform, and so-called elephant flows (large files) are more efficiently transported through a dedicated circuit than a series packets and packet switches. An OpenFlow controller can route the flows appropriately. For signal processing, both the compute resources and the transport resources can be load balanced with low overhead using circuit switching. Figure 4 illustrates the results of an Intel study on chip level circuit switched communication networks for mesh architectured multicore chips.

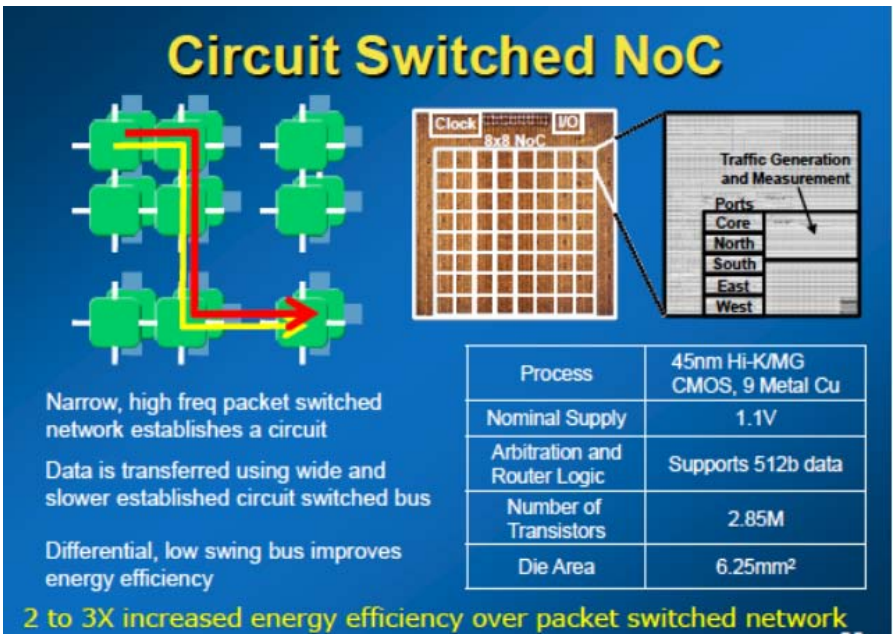

Figure 4. Network-on-chip is an emerging architecture for parallel processors. (Courtesy of Shekhar Borkar, Intel)

An optical matrix switch consisting of an array of Mach Zehnder switches is shown in Figure 5. These switches have enormous advantages in transport latency, energy and capacity over packet switches. System level benefits have been estimated to be i) a 10^3 reduction in cost; ii) a 10^3 increase in data rate; iii) optimal tradeoff of energy and latency; iv) maximization of resource utilization, capacity, interoperability, and control.

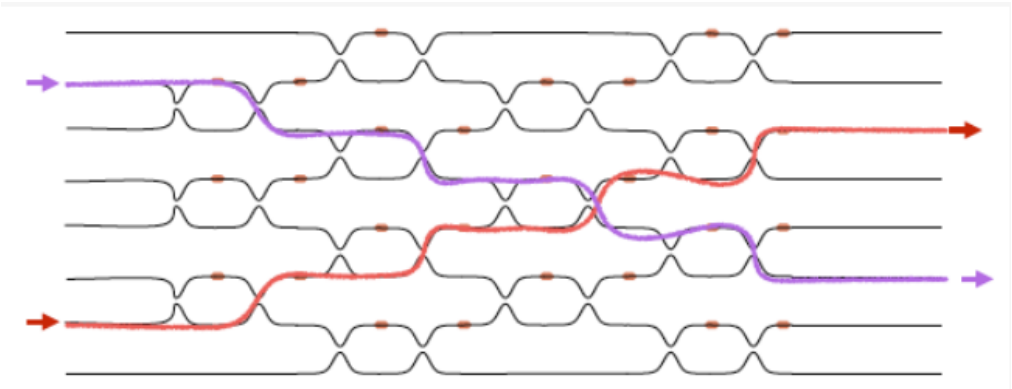

Figure 5. An Optical Path matrix switch for transporting large 'elephant' flows in networks. Shown is an 8x8 Mach Zehnder array. (compliments of Shu Namiki, AIST, VICTORIES Project, Japan)

The general trends for photonic interconnects, switches and routers are shown in the temporally coarse roadmap of key components and attributes in Figure 6.

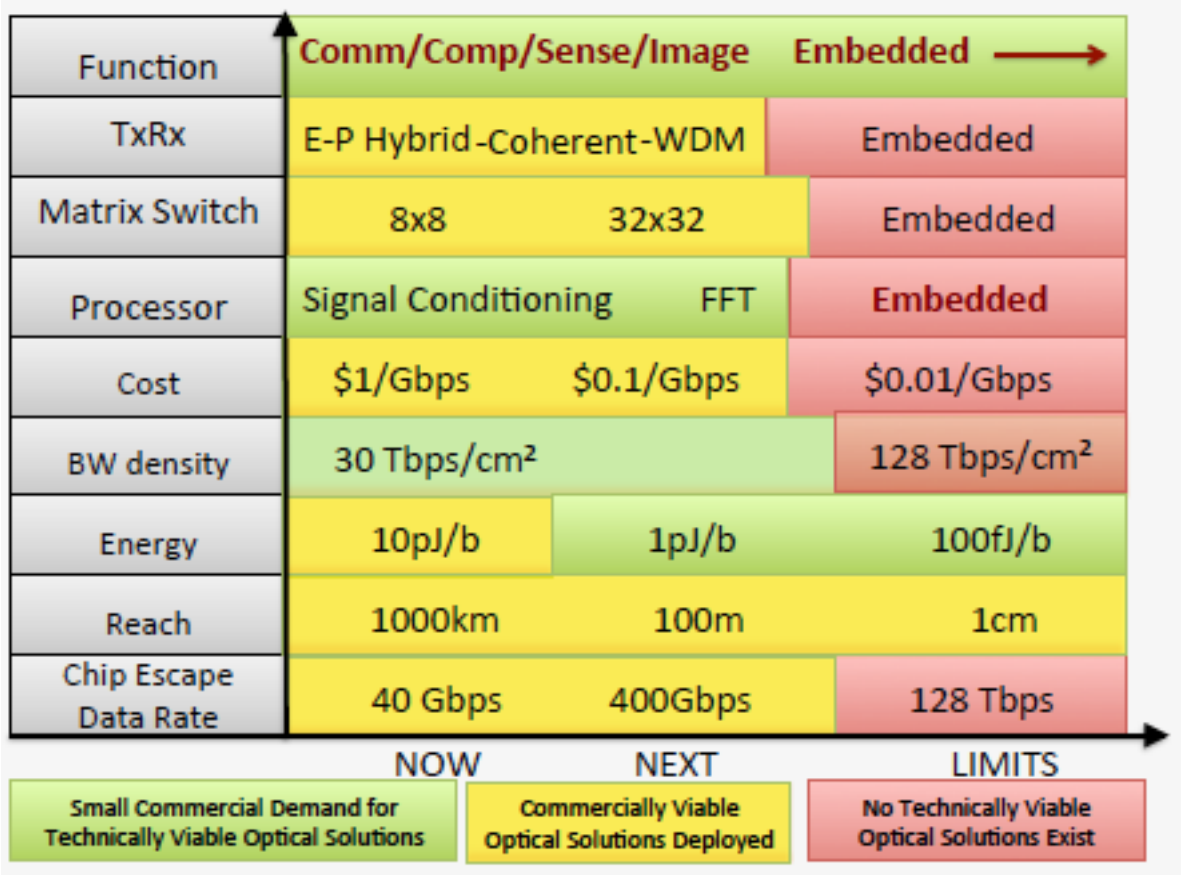

Figure 6. System level trend: the stand alone transceiver will become embedded to provide seamless, system-wide photonic interconnection with the current subsystem architecture dissolving into optimized and distributed electronic and photonic circuit elements.

THE MONOLITHIC INTEGRATION PLATFORM

WAFER SUBSTRATE MATERIAL

The wafer substrate material and the photonic integration architecture define the transceiver manufacturing platform and manufacturing capacity. Three wafer materials platforms are used today: GaAs, InP and Si. For MM vertical integration, GaAs-based VCSEL arrays are used. For SM planar integration, the two wafer platforms are InP and Si. Initially, only the need for long reach in telecommunication networks dictated the use of the more costly SM the transmission mode. Today, integrated planar photonic circuits in InP are providing bandwidth density scaling that is justifying a technology transition from vertical to planar integration. The small size on InP wafers, typically 100mm in diameter, limits ultimate production volume and cost reduction. The Si wafer platform is used in foundry-level production with standard CMOS IC process tools on 200mm and 300mm wafer diameter

platforms. For high volume production, > 1 million chips, the silicon wafer provides the only platform capable of meeting the yield and volume projections.

TRANSMISSION MODE

Multi-Mode Links with directly modulated vertical cavity lasers

Multimode links are the standard for datacom applications today. The low threshold current of the VCSEL laser, the high efficiency of direct modulation, and the low cost of wide tolerance, multimode fiber connects make this platform the choice for high volume, cost sensitive applications. Data rate is limited to ~25 Gb/s by direct modulation of VCSELs and by reliability. The short cavity length and wide divergence of VCSEL lasers dictates MM transmission that makes bandwidth density enhancement with phase modulation and WDM difficult. The vertical coupling and single channel transmission facilitate chip stacking on silicon ICs for electronic control and for redundancy and switching applications, as shown in Figure 7.

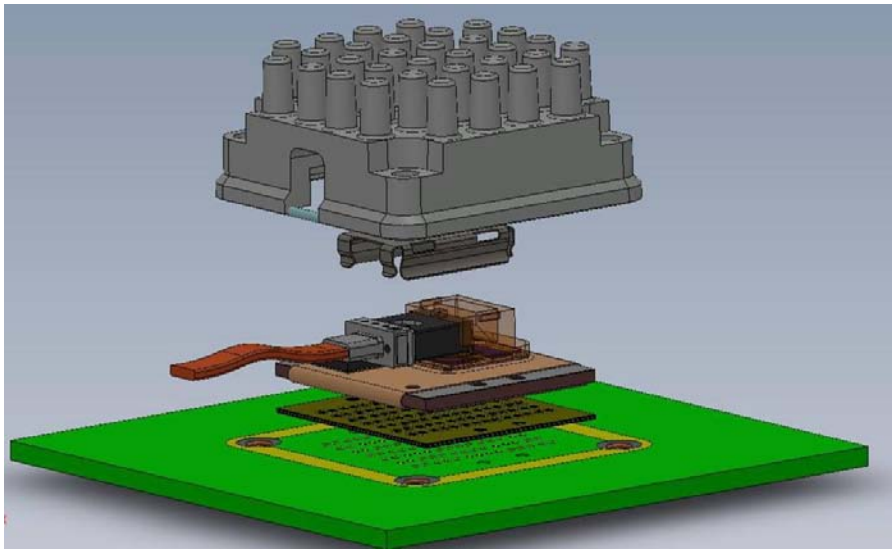

Figure 7. High-yield arrays of parallel GaAs VCSELs, PIN photodetectors, IC drivers and fiber connects provide short electrical traces and low cost MM parallel fiber alignment. (image compliments of Finisar)

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Single-Mode Links: edge emitting lasers with external modulators

Today, InP-based PIC module transmitters and receivers are the core "optical engines" that power the telecom network. Future generations of PICs will capitalize on the semiconductor learning curve of earlier generations to further enable the scaling to multi-Tb/s devices. This scaling path for integrated photonic chips will require significant innovation in chip, packaging, and assembly technologies. In the future, the demanding performance of these systems and "engines" will be enabled by leveraging established capabilities from the electronic IC ecosystem.

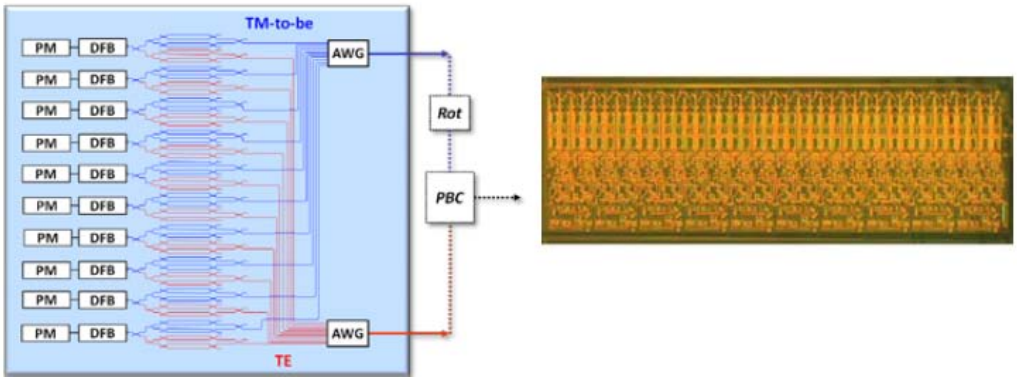

Figure 8. Schematic diagram of an InP-based 500Gb/s PM-QPSK transmitter PIC and the active block PIC on the right. The active block contains 10 tunable distributed feedback lasers, 40 Mach-Zehnder modulators, and all required sense and control electronics. (compliments of Fred Kish, Infinera)

WAVEGUIDES, FILTERS AND PASSIVE DEVICES

Optical waveguides are being increasingly implemented to meet distributed system requirements for transmission lines for intra-chip, intra-package, board-level and backplane signaling. The 'skin effect' increases resistance and loss for electronic transmission through copper wires at high single channel data rates, because high frequency signals are expelled from the conductor. This property of electronic transmission limits the scaling of interconnection bandwidth with two major consequences: i) the interconnect design rule for copper transmission media is 20dB loss; and ii) improved and more expensive Cu and associated insulation materials are required to reach required performance. For single mode (SM) transmission photonic waveguide interconnects offer strong confinement, low loss and wavelength division multiplexing of >100 signal channels. **As bandwidth density requirements increase, photonic waveguides favorably compete in cost and performance.**

The silicon platform is uniquely capable of delivering high transparency and high index contrast in the 1200-2000nm wavelength range. This range is ultimately constrained by the transparency of both the core (Si) and the cladding (SiO_2).

Table 3. Integrated Waveguide Roadmap

Key Attribute	Parameter	Description	*2016*	*2018*	*2020*	*2025*	*2035*
Transparency	dB/cm	attenuation/distance	0.35	0.1	0.05	0.001	0.001
Material	n	effective index	1.8-4	1.8-4	1.8-4	1.8-4.	1.8-4.
Index Contrast	Δn	n(core) - n(clad)	10^{-3}-3	10^{-3}-3	10^{-3}-3	10^{-3}-3	10^{-3}-3
Stability	pm/^{o}K	spectral shift of resonator	*25*	*1*	*1*	*0.5*	*0.01*
Power	mW	optical power capacity	30mW	30mW	50mW	100mW	500mW
Wafer Uniformity	nm	layer thickness variation	10nm	1nm	1nm	0.5nm	0.5nm
Material System	Core /Clad	waveguide and clad materials	Si,SiN /SiO_2	Si,SiN, Ge,ChG /polymer, SiO_2,ChG	multilayer	multilayer	multilayer

The targeted implementation of silicon photonics is monolithic integration of optical circuits with electronic circuits in a "CMOS-like" standard process flow, as shown schematically in Figure 9. The historical path to monolithic integration began with discrete breadboards, then hybrid packages and chips, and finally monolithic integration. Current commercial products feature monolithic modulator-waveguide-detector integration with hybrid flip-chip bonding of the laser and electronics. The laser is the most difficult device to monolithically integrate on a silicon chip, and III–V light emitters have been hybrid-integrated with transparent adhesives or wafer bonding in the back-end-of-line (BEOL). Monolithic electronic-photonic integration in silicon is expected to enable scaling of cost, manufacturing volume, power dissipation, and bandwidth density. Silicon CMOS process technology is one of the most elaborate human-made resources in history. It provides the most accurate yet cost-effective processing for monolithic integration of electronics and photonics on a chip. The fundamental challenge for CMOS process technology for Si photonics is dimensional tolerance, because wavelength-dependent optical devices are more dimensionally sensitive than transistors. Fabrication errors in waveguide width/thickness as small as 1 nm can be consequential for on-chip DWDM. The absolute process tolerance of reduced index contrast designs should be larger because of weaker confinement of light modes than in high index contrast designs. The drawback of Si_3N_4 materials deposited by chemical vapor deposition is residual hydrogen in the film, leading to strong N–H bond absorption near 1520 nm, which is at the middle of the optical communication wavelength range. Annealing at 1100C or higher is necessary to remove hydrogen from SiN_x layers, and these temperatures are not tolerable in the CMOS BEOL processing. However, it should be noted that Si_3N_4 deposited by PVD is a compatible process that introduces no hydrogen.

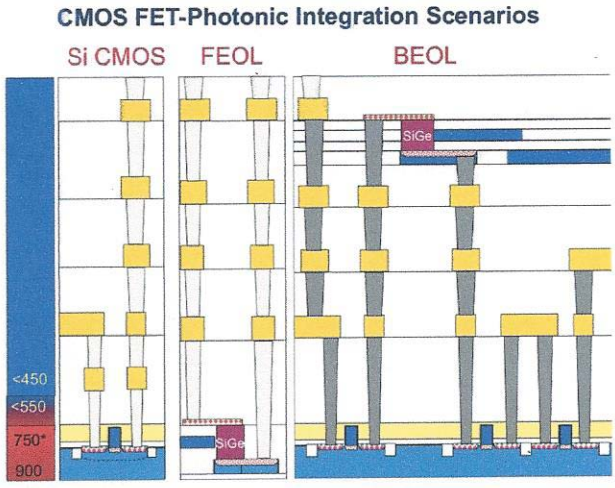

Figure 9. Monolithic integration of active and passive photonic devices in a silicon CMOS process can be considered for insertion into (a) FEOL process regime where high temperature CVD processes can be supported and (b) BEOL interconnect stack with the development of low process temperatures and materials.

Scaling interconnection to the highest bandwidth density will necessarily utilize DWDM wavelength division multiplexing of > 100 channels/waveguide. Dimensional scaling for silicon photonics is dependent on the index difference (Δn) between the core and clad materials. SiO_2 is the clad material for silicon photonics. The optical device footprint can be scaled smaller as the index contrast Δn increases; but device fabrication tolerances, such as waveguide sidewall roughness, become more demanding. Table 1 compares athermal designs for two waveguide core materials: Si and Si_3N_4. Utilizing a negative

thermo-optic polymer clad, the composite waveguide materials systems exhibit thermally stable optical filter functionality: zero resonant wavelength change between 0–70C for DWDM applications where 50 GHz (0.4 nm) channel spacing is typical.

Table 4. Polymer clad composite waveguide materials systems for thermally stable optical filters: zero resonant wavelength change between 0-70C for Si and Si_3N_4 cores.

Material	n	Γ	n_{eff}	n_g	R_b (μm)
Si	3.48	0.58	1.78	3.68	3.5
Si_3N_4	2.05	0.9	1.75	2.2	5.5

Note: Core refractive index (n), optical mode confinement factor (Γ), effective index (n_{eff}), group index (n_g), and minimum bend radius (R_b).

Enhanced spectral efficiency (bit/Hz) is a currently commercially deployed alternative to DWDM for high bandwidth density. Quadrature optical phase shift keying (QPSK) with electronic digital signal processors silicon MZI modulators with advanced CMOS technology has been commercially deployed (Cisco Systems announced a 100G CFP module in the Optical Fiber Conference [OFC] 2013, and Acacia Communications announced in OFC 2014). QSPK provides higher spectral efficiency in terms of bits/Hz by modulating the phase of the light, with specified phase delays, as well as the traditional light intensity (OOK, on-off keying). A signal with the same amplitude modulation frequency can be multiplexed into time-domain and phase-domain encoded channels. The challenge of on-chip and on-module dimensional precision and thermal stability for WDM and DWDM has been noted. Athermalization using a composite silicon-polymer waveguide can achieve 0.5 pm/C resonant wavelength stability that is capable of 220 wavelength channels in the communication C-band near 1550 nm. The reduced confinement of the optical mode allows a higher power transmission limit for the waveguide, and the channel number achievable by athermalization can be more than 10 times that normally handled in Si photonic waveguides. The addition of a thin, photosensitive As_2S_3 chalcogenide glass (ChG) layer between the negative TOC polymer and positive TOC silicon, as in Figure 10 , adds a resonance trimming capability to the filter, since an index change is optically equivalent to a dimensional change.

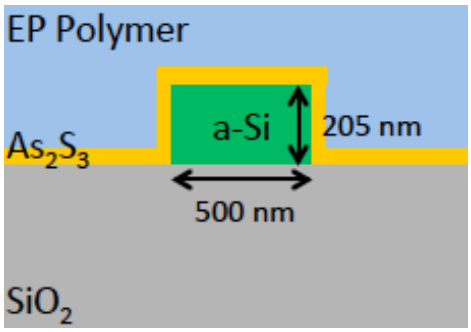

Figure 10. Athermal and trimmable design for silicon waveguides.

Engineering mode sharing between the core(+ thermo-optic) and the clad (– thermo-optic) results in thermal stability for add-drop fi lters of 0.5 pm/K. The thin As_2S_3 layer provides a compatible photosensitive index for precision resonant wavelength trimming.

PHOTODETECTORS

The materials selection for integrated waveguides is based on the following parameters:

- absorption
- dark current
- process integration

Germanium growth without a thick graded buffer layer and dislocation-free Ge in selective area epitaxy on Si are essential to waveguide-integrated optical devices. Because of the built-in biaxial tensile strain in Ge-on-Si following growth, the absorption edge is red-shifted to beyond 1600 nm, which is beneficial for detection of C+L bands (wavelength channels allocated for standard wavelength division multiplexed communication [C-band] and extended longer wavelength communication [L-band]) of optical fiber communication. Selective area epitaxy with SiO_2 masking allows submicron wide Ge stripes to be directly integrated on the waveguide. For an optical layer in the BEOL interconnect stack, Ge on a non-crystalline substrate such as SiO_2 or amorphous Si must be developed. There have been two approaches reported: polycrystalline Ge melting/solidification growth on SiO_2 in the front-end-of-line and Ge on amorphous SiO_2 passivation layers and/or amorphous Si waveguides. Both approaches are quite promising for monolithic integration.

Table 5. Photodetector integration roadmap

Key Attribute	Parameter	Description	*2016*	*2018*	*2020*	*2025*	*2035*
Absorption	α (cm^{-1})	loss @ 1550nm	10^3	10^4	10^4	10^4	10^4
Dark Current	I (nA)	interface + bulk	0.2	0.1	0.1	0.1	0.1
Process Integration	cm^{-2}	dislocation density	10^7	10^7	10^6	$<10^5$	0
Efficiency (p-i-n)	R (A/W)	responsivity	1	1.1	1.1	1.1	1.1
Bandwidth (p-i-n)	B (GHz)	B @ 1550nm	40	67	100	100	100
Gain x Bandwidth (APD)	GB (GHz)	GB @ 1550nm	300	400	--	--	--
Guided Power	mW	~linear response	30mW	100mW	100mW	100mW	100mW

MODULATORS

The materials selection for integrated waveguides is based on the following parameters:

- electro-optic coefficient
- insertion loss
- extinction ratio
- spectral range
- process integration

Silicon modulators Electro-optic modulators based on electro-refractive (ER) and electro-absorptive (EA) effects have been reported. Ring resonator and Mach Zehnder (MZI) modulators (ER) have been demonstrated. Si rings showed a higher bandwidth density and smaller energy/bit. The drawback is the previously described sensitivity to thermal fluctuations. Currently, thermal heater control of the ring modulators is employed to stabilize the operation and to precisely tune the modulation wavelength with an added power penalty that depends on data rate. Silicon MZI modulators use standard junction or MOS process technology and are uniquely capable of QAM phase shift coding. Dual polarization with 16 QAM coding have achieved spectral efficiencies of 8 b/Hz for single channel data rates of 226 Gb/s.

While the bandwidth density for advanced modulation formats is he requirement for energy hungry DSP decoding circuitry.

Germanium modulators The Franz-Keldysh (FK) GeSi electro-absorption modulator (EAM) has been demonstrated for operation at λ =1550 nm. The dilute alloying of Ge with Si moves the absorption edge of as-grown, tensile-strained SiGe to 1550 nm. The FK EA modulator should provide the lowest energy/bit performance because of its reverse bias field-only operation. The major issue in device design is the reduction of the operating voltage to CMOS power supply levels of <1V. A compressive-strained Ge-based EAM for wavelengths shorter than 1550 nm based on the quantum confined Stark effect (QCSE), which is an electric field induced energy shift in the absorption edge in semiconductor quantum well structures, has been proposed and demonstrated. Operation of this QCSE modulator near 1260 nm (the communication O-band) would have significant value if its process complexity could be reduced.

Table 6. Modulator integration roadmap

Key Attribute	Parameter	Description	*2016*	*2018*	*2020*	*2025*	*2035*
Baud Rate	Gb/s	OOK rate	25	50	50	100	100
ExtinctionRatio/InsertionLoss	dB/dB	$\Delta\alpha/\alpha$	2	2.5	3	--	--
Spectral Range	nm	@ $\Delta\alpha/\alpha$ spec	*25*	*25*	*25*	*25*	*25*
Spectral Efficiency	b/Hz	DP-QAM	2	2	4	8	8

LASERS, GAIN BLOCKS AND OPTICAL SWITCHES

Monolithic germanium gain blocks Germanium is an indirect semiconductor with a Γ-L valley separation of 140 meV. Photons are most efficiently generated at the Γ-point (direct gap position) where no change in wave vector is required. As the energy position of the conduction minimum at the direct gap wave vector (Γ-point) is lowered and approaches the minimum for the band structure at L (indirect gap position), photon emission for lasing becomes faster and the preferred recombination pathway for the forward-biased injected carrier density to approach equilibrium. This small energy separation together with tensile strain-engineering allows for electrons to populate in the Γ valley under n-type doping. Approximately 0.2% tensile-strain is typically present in Ge-on-Si epilayers due to the thermal expansion mismatch between Ge and Si. This level of strain will shrink the Γ-L valley separation to 110 meV and allow net positive gain when doped at a donor concentration $N_D > 5x10^{19}$ cm^3. Ge laser devices have been demonstrated by optical pumping and electrical injection. The current challenge is to reduce the lasing threshold current.

Device structures External cavity lasers with waveguide integrated gain media are favored for integrated light sources because of all optical power is waveguide coupled and because temperature tuning of the emission wavelength can be achieved due to the high thermo-optic coefficient of silicon.

Bond-and-process layers for individual laser devices can be integrated into contact layers and evanescently self-align-coupled to waveguides. The key design issues for these structures are i) thermal stability over 0<T<100C and modal overlap of the gain medium with the waveguide; ii) manufacturing yield; and iii) operational reliability. For most failure modes, reliability increases with emission wavelength, favoring 1550nm emitters.

Design Rule Tradeoffs Packaging cost and chip functionality determine the light source integration strategy. Low loss coupling to fiber will enable low manufacturing cost. For transceiver and

optical engine applications, integration of 1-12 lasers may have sufficient yield for low volume applications, but it is not likely to be a significant cost factor relative to ASIC and fiber-coupler integration. When electronic-photonic synergy is required, such as in optical networks for 1K multicore chips/packages, thousands of monolithically integrated lasers are key to the network architecture.

For large optical matrix switches, ubiquitous gain block integration within Mach Zehnder arrays is essential for scaling port count. Until monolithic gain blocks are available the tradeoff between optically pumped waveguide amplifiers and semiconductor optical amplifiers will be determined by performance (noise figure, footprint and gain/cm).

When single mode chip-to-chip coupling becomes cost effective, regulated wall plug light sources may be architecturally favored for applications such as data centers where photons are everywhere and light source stability is critical. This optical power supply architecture would be a major advance in flattening distributed systems by eliminating tiers in the interconnection interconnection hierarchy shown in Figure 11.

The design rules for laser, gain block and optical switch integration include the following parameters.

Table 7. Laser, Gain Block, Optical Switch integration roadmap

Key Attribute	Parameter	Description	*2016*	*2018*	*2020*	*2025*	*2035*
Coupled Power	mW	waveguide coupled	1	5	20	30	30
Spectral Range	nm	1200, 1310, 1550	+/-10	+/-10	+/-10	+/-10	+/-10
Temperature Stability	pm/K, mW/K	wavelength, power	*5*	*1*	*1*	*0.5*	*0.01*
Package Integration	optical power supply	wall plug, package or waveguide integration	*2D ext*	*2D ext*	*2D hybrid*	*regulated wall plug*	e-p monolithic
Reliability	MTTF (hrs)	component life	10^4	10^4	$3x10^4$	$3x10^4$	10^5

ISOLATORS

The design rules for integrated optical isolators are based on the following parameters:

- transparency
- magneto-optic coefficient
- insertion loss
- spectral range

Monolithic optical isolators The layer-by-layer processing that is inherent to the Si CMOS platform enables buffer-assisted deposition for enhanced phase stability and device functionality. A good application of this principle is the ring-resonant optical isolator. The magneto-optical cerium-doped yttrium-iron-garnet (YIG) material provides a Faraday-effect-induced non-reciprocal transmission medium. The device presents different indices of refraction (resonant wavelengths) to launched and reflected signals, and the resonator acts as an optical diode. A layer of YIG-on-Si stabilizes Ce:YIG against phase separation and preserves its optical non-reciprocity. The optical resonator structure gives field concentration and enhanced effective interaction length, and Ce:YIG on one side of the “racetrack” resonator discriminates against the direction of optical signal transmission. The result is an isolator device with the smallest footprint ever and a high performance □ 20 dB isolation at □1550 nm. The ability to design and process multilayer composite waveguide structures adds unique value to the Si photonics platform that is not accessible elsewhere. The examples discussed for athermal optical filters,

trimmable resonant wavelengths, and optical isolation are only the beginning of the exploitation of optical performance scaling with composite materials structures.

APPLICATION DEPENDENCIES

Photonics is an analog signal processing platform that has been adapted to digital for communication and computing. Optical Signal Processing promises high functionality with low power and latency. The OSP is a special purpose processor for applications such as QAM Phase Shift Keying, Fast Fourier Transforms, Channelizing or RF radio. For these analog applications, signal to noise ratio and linearity are the primary determinants in design. The system performance metrics are Spurious-Free Dynamic Range (SFDR), Noise Figure (NF) and Gain. Coherent detection, used to enhance system performance, is a good example that requires specialized integration schemes.

Consider an RF-photonic 400 filter channelizer system-on-chip that is executed within a 20mmx25mm reticle. Encoding the RF signal on the optical carrier requires integrated linear modulators with waveguide loss <1dB/cm. For high S/N, Power Handling and Linearity are more important than Bandwidth. Uniquely, a low RIN noise (Relative Intensity Noise) signal laser is important and may require a specialized wall plug light source configuration. The RF signal frequencies are relatively low for photonic modulation, and the signal is unlikely to degrade during optical transport. Silicon photonic integration of the filter and modulator circuits has been demonstrated, and achievement of an SFDR value of 118 dB*Hz is considered reasonable with a low RIN laser.

PROCESS INTEGRATION FOR ELECTRONIC-PHOTONIC ICS

ULSI Electronic-Photonics A metal wire communication channel has poor power efficiency due to i) loss: primarily resistance and line capacitance and ii) limited bandwidth density: skin effect and EMI at high frequencies. Scaling power efficiency with metal interconnection equates to reducing wire length or reducing signal integrity, and limiting bandwidth density. Metal wires ‘hit-the-wall’ when the spatial crowding consequence of reduced wire length conflict with the high data rate requirement of increased bandwidth density. Photon transport does not possess the significant distant-dependent loss mechanisms of wires; and the non-interactive nature of photons allows communication channel multiplexing in a single fiber (wavelength division multiplexing, WDM). The benefits of photonic interconnection relative to metal wires are lower power dissipation, longer reach, higher bandwidth density and lower bit error rate.

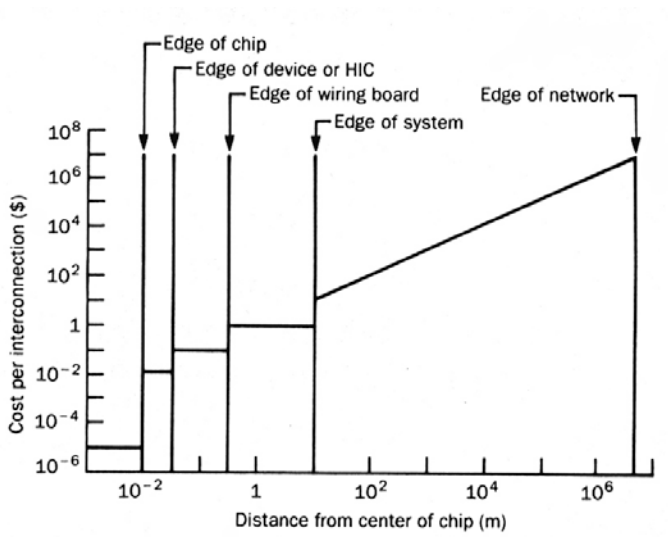

Figure 11. Cost vs. length for the interconnection hierarchy. (John Mayo, ATT Bell Labs, 1989).

At each interface, bandwidth is aggregated, and energy and cost are expended. Initially introduced for >100km (network) telecommunication, fiber optic cables are today deployed at much short lengths, 5cm (board), in highly parallel computing systems.

Figure 11 gives a schematic view of the interconnection hierarchy. Although the data are ~30 years old, the message has stayed the same: i) interfaces are costly; and ii) integration is the most powerful solution to scaling communication. Optical fiber with wavelength division multiplexed lines (multichannel integration on fiber) transformed telecommunication into the Internet. Parallelism, from the network 'cloud' to the multicore chip, has rebalanced the system performance load toward communication, and interconnection at every level of the hierarchy is being reconsidered.

System scaling for metal interconnection

The energy of data transport is becoming larger than the central processing component as systems approach 'exascale' FLOP/s and B/s. As an example, 200x more energy is needed to transport a bit to a nearest-neighbor chip than is required to operate on it. Across a 50m, multi-stage network, with routers and multiple transceiver hops, the factor may become 1000x. The projected energy for a FLOP (2015) is 0.05-0.1 pJ/bit. The projected energy for data transport (2015) is 2-10 pJ/bit. The power budget for a typical electrical link includes ~20-25 dB loss (>99%) between the transmitter and the receiver. Photonic communication at the board level has become a UHPC system design rule. The implementation of intra-chip photonic communication will be driven by i) a saturation of power efficiency scaling for metal at short distances, and ii) the WDM bandwidth density advantage of photonics.

Chip-level scaling for metal interconnection

The energy efficiency of metal wires on chip will saturate at 100fJ/bit (currently ~1pJ/bit). The loss associated with metal conductors requires installation of repeaters to amplify and condition the signal at a penalty of about 50fJ/bit/mm or 500fJ/bit for 10mm interconnect. The best equalized/low-swing wires can reach 200fJ/bit for 10mm interconnects. The smaller wire diameter at later CMOS technology nodes will require as many as 10 repeaters to traverse 1mm, but the reduced energy/transistor is projected to yield constant energy/bit. Energy requirements are mostly dominated by wire capacitance (not diameter, but fringe and wall-to-wall capacitance) that scales only with distance. For single

channel, multimode waveguide transmission, photonics offers little advantage for chip-level data transport. However, single mode, WDM photonics can give >100x advantage in bandwidth density and power efficiency for global, chip-level interconnection. At 4um pitch and 1Tb/s/waveguide optical communication provides 250Gb/s/um. When compared to the metal density of ~3-4Gb/s/um (optimal energy design), a 60-80x bandwidth density advantage is achieved.

Scaling of monolithic, intrachip photonic interconnection

Electronic-Photonic (E-P) integration can provide disruptive improvements in the energy-delay performance for signal processing and new circuit functionality by smart partitioning among E-P components. While hybrid integration may allow near term 'bread-boarding' of E-P systems, only monolithic integration in CMOS can provide the scalable performance: i) by enabling reduced parasitic capacitance with smaller sized, higher density, waveguide-integrated components; and ii) by enabling high E-P circuit complexity for new functionality. Current photonic cables at the board and system level are VCSEL-based, multimode, single channel fiber connects. When bandwidth density requirements dictate WDM architectures, the traditional board-edge E-O-E transceiver interface will give way to single mode, chip-level photonics. Monolithic Ge-on-Si microphotonics can provide the necessary suite of CMOS-integrated photonic devices.

Fabrication of silicon microphotonic devices can occur within the same process sequence as the CMOS flow and can minimize the requirement for additional mask levels, as shown in Figures 9 and 10. Today, microphotonic integration is implemented in the transistor plane at the front end of the line (FEOL). As transistors scale to sub-10nm dimensions, photonic devices dimensioned at λ/n (wavelength/index) ~500nm, will occupy too much area, and the monolithic photonic plane will move into BEOL interconnect stack. This BEOL architecture could yield a significant reduction in process complexity, if the higher bandwidth of the photonic layer triggers elimination of metal interconnect layers. The 180nm CMOS process node is sufficient to fabricate current microphotonic components. The integrated process flow developed for the BAE Systems, Manassas fab is described in the following text. The detailed steps required for CMOS electronics are assumed in the flow and omitted for here simplification.

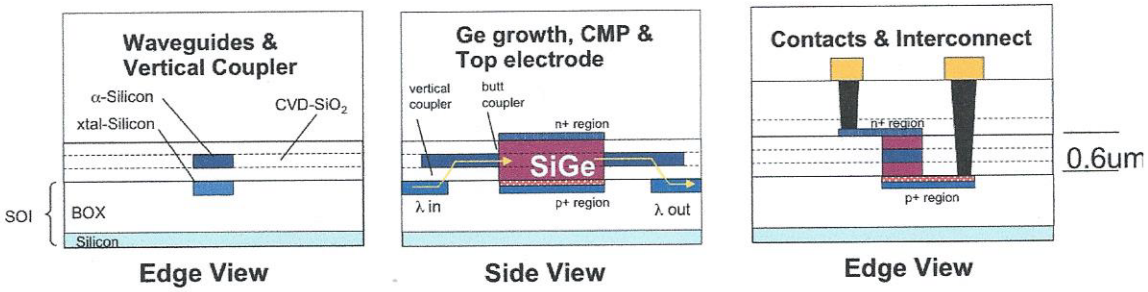

Figure 12. Summary of FEOL SOI microphotonic device fabrication sequence.

A schematic view of the FEOL process sequence to fabricate photonic devices is shown in Figure 12. The major steps include: i) optical waveguide fabrication for routers, filters and couplers; ii) electrode formation, growth and planarization of germanium and iii) contact and interconnect metallization. The sequence is described briefly below.

SOI Layer Thickness For a single TE mode optical waveguide, the silicon layer thickness is 200nm for channel waveguides. SOI substrates can be provided with 3.0 μm bottom oxide thickness; however the silicon thickness it typically 270-280nm thick. Thinning can be achieved thermal oxidation in a furnace followed by removal of the oxide with a wet etch with dilute hydrofluoric acid.

N_{well} and P_{well} Implants Early in the CMOS process, a sacrificial oxide is deposited to set up for the n^+ and p^+ well regions supporting the electronics. Well implant doses exceed requirements for the Ge p-i-n diodes used for modulators and detectors, but they are consistent with the Ge laser device requirements.

Level-1 Waveguides After silicon surface preparation (compatible for transistor devices regions with pad oxide and nitride depositions), the level-1 waveguides are formed using the same shallow trench isolation (STI) process used for electrical isolation. Additional steps are added for sidewall smoothing of the waveguides. A CMOS standard clean (SC) wet etch can be used for smoothing by chemical oxidation. The remaining trenches are filled with additional oxide and planarized to the nitride.

Gate Formation and P-carrier Implants The transistor gate oxide is formed via thermal oxidation of exposed silicon regions following removal of the sacrificial oxides. Gate oxide thicknesses are typically 26Å for this 180nm technology node. LPCVD polysilicon (t=250nm) is deposited and etched to form the transistor gate electrodes. Implants for lightly doped drains, I_{dd}, use sequential resist masked processes for p-type and n-type regions. The I_{dd} p-type implant dose of boron is used for the vertical p-i-n photodetectors and modulators. Activation of the implant yields a concentration of $1x10^{19}$ cm^{-3} for low resistivity contacts to the photonic devices.

Sidewall spacers are formed on the polysilicon gate electrodes using a deposited conformal oxide followed by an anisotropic reactive ion etch. Graded junction implants for n^+ and p^+ regions are then formed for transistors followed by deposition of a capping oxide and source/drain anneal. Salicided junctions of $CoSi_2$ are formed using sputter deposited cobalt reacted with silicon in masked source drain regions of the transistors. Contact windows are defined for active photonic devices to utilize the same process. $TiSi_2$ can also be used for risk mitigation of cross contamination with subsequent germanium CVD processes.

Level-2 Waveguides Formation of butt coupled silicon waveguides for optical impedance matching to germanium devices requires the insertion of a level-2 waveguide. An amorphous silicon film deposited by PECVD is used for the waveguide layer. A dual layer stack of 200nm PECVD TEOS oxide followed by 200nm PECVD a-Si is formed. The 200nm oxide film defines the coupling gap used for evanescently coupling light vertically from the first level SOI waveguide to the PECVD silicon local waveguide, as shown in Fig. 3. The PECVD silicon waveguides are formed using RIE silicon etch. After etching the PECVD silicon waveguides, a 300nm HDPCVD oxide layer is deposited followed by oxide CMP defining a total stack height of 600nm. The planarized stack is then capped with a thin LPCVD silicon nitride film.

GeSi Selective Epitaxy The oxide/silicon/oxide stack is then patterned and etched forming trenches for the GeSi modulator and photodetector devices. The exposed regions of the stack are etched using a reactive ion etch process for silicon oxide. A GeSi alloy with 0-0.8% silicon, supporting both modulator and photodetector devices, is epitaxially over grown in trenches (see Figure 11).

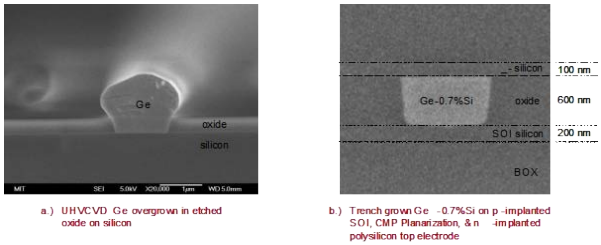

Figure 13. Selective, trench filled germanium processing: a) germanium overgrown in patterned oxide trenches on silicon and b) process integrated structure of a p-i-n diode using germanium-0.7%silicon alloy on SOI substrate.

GeSi p-i-n Diode Top Electrode After germanium overgrowth in the trenches, the film is planarized to the oxide layer using a modified CMP process. After CMP and cleaning, a 100nm thick PECVD a-silicon film is deposited for the top electrode. The film is then doped with the equivalent of an n-type I_{dd} implant of arsenic. The target carrier concentration is 10^{19} cm^{-3}. The film is patterned and etched using a silicon RIE process.

BEOL Interconnection With the completion of the top electrode for Ge devices, all of the major photonic components have been defined within a 610nm height above the silicon layer containing all electronics (see Figure 14). Completion of the pre-metal dielectric layer with the deposition of an undoped HDPCVD oxide defines the required contact height. The height for metal contacts in the 180nm CMOS technology node is 1.0 micron and defines the position of the first metal layer of interconnect. The 180nm CMOS process defines interconnect with 6 levels of metal comprised of 4 levels for local interconnect and 2 levels for the global interconnect. For monolithic BEOL microphotonics, the same dimensions and processes are relevant with the constraint that process temperatures remain below 450C.

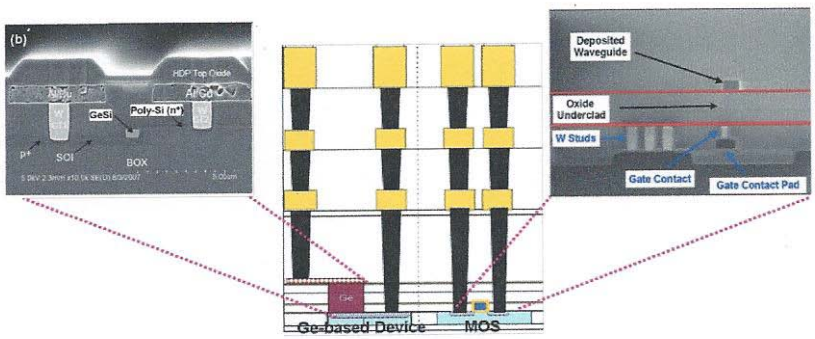

Figure 14. Monolithic integration of photonic and electronic devices using silicon CMOS processes. Integration of germanium for active photonic devices is uses a temperature tolerant FEOL process and a temperature constrained (T<450C) BEOL process.

Scaling Microprocessor Architecture The physics of information processing and transport dictates an ultimate tradeoff between clock/communication frequency and parallelism. While aggregate bandwidth must continue to scale at all levels of the interconnection hierarchy, the data rates of each channel must reach an asymptotic limit defined by the dissipated power density. Monolithic waveguide integration provides a path for scaling to small photonic devices coupled with low parasitic capacitance to electronic drivers and receivers. Dimensional scaling will allow many generations of microprocessor core count increases, following Moore's Law. However, massive parallelism requires new algorithms to

divide the problem for efficient computation and new hardware to communicate among the cores. These tools have begun as remnants of the single CPU paradigm, and the actual FLOP/s is only a small fraction of the potential FLOP/s (#cores x FLOP/s/core).

Microprocessor performance is being gated by two factors: communication bandwidth and programmability. Bandwidth is needed to coordinate signal processing among the compute nodes without delays associated with bus contention. As the number of cores, N, grows exponentially with time, the desired communication bandwidth must grow as N^2. Commercial multicore processors use a bus interconnect; communication occurs *implicitly* through memory; and core count is limited by the low bandwidth and high loss of the long metal bus line. Figure 6a shows a mesh interconnection solution, where data is transported point-to-point between nearest-neighbor cores. The mesh architecture enables hundreds of cores to communicate with inexpensive local communication, before contention and distance-dependent routing energy become limits. However, the mesh introduces heterogeneity that increases programming complexity by requiring locality in the lines of code for point-to-point coordination of thousands of processes. Broadcast communication can relieve the need for locality in programming, but it is slow and power inefficient on an electrical mesh. A broadcast photonic network can provide high bandwidth, low latency and power efficient communication among cores with no routing requirement by the hardware or data locality in the lines of code. This parallel architecture is known as ATAC: All-to-All Computing.

ROADMAP OF QUANTIFIED KEY ATTRIBUTE NEEDS

The Cost Driver Information system hardware is transitioning to higher photonic component content. As baud rates increase on shorter reach links, optical transmission methods are better able to meet (energy x delay) targets than conventional electrical transmission. As optical interconnect links become shorter, photonics assumes a larger part of the total interconnect count and a larger fraction of system cost. As system parallelism increases traditional routed, packet switched architectures are migrating back to bus-based, circuit switched networks. *Convergence-for-Cost* will favor high bandwidth density, low cost solutions that maximize signal integrity with minimal signal processing. The immediate implementation utilizes the current architectural and software infrastructure with a dependence on CMOS scaling for cost and power efficiency competitiveness. This path will migrate to a system level *Convergence-for-Cost* design paradigm that is grounded on cost-per-function rather than cost-per-component.

The Energy Driver The total energy consumption by IT in developed economies is approximately 5% of the electrical power generation today and will approach an unsustainable 10% over the next decade if better solutions to meet growing capacity demand are not developed. In Japan, a METI report projects that network IP switches could consume 100% of electrical power generation between 2020-2035 depending on CMOS scaling performance. Data Centers consume 6MW of communication power (Dorren), mostly in switches. Google data centers consume >100MW (with nearly 50% for infrastructure support). Apple's data center in North Carolina requires more than 20MW. NSA's facility in Utah specifies a power requirement of 65MW (equal to all of the homes in Salt Lake City). In 2009 a typical telecom carrier consumed 7 TWhr of electricity with a growth rate of 5%/yr. AT&T's network traffic was >10 PB/day. In 2012 the

Internet node in The Netherlands transmitted 15 PB/day and 4.1 EB/yr (40% higher than 2011); port count has grown at a rate of 70%/yr over the past decade.

The Fundamental Limits of Density: high and low Basic physics dictates that information system architectures migrate to parallel, lower baud rate designs to deliver scalable (energy x delay) performance. This architecture migration has enabled compute system performance in FLOPS to grow at a rate of 100% CAGR (1000x/10yr) while the underlying microprocessor chip performance followed a slower Moore's Law at 50% CAGR (100x/10yr). Communication protocol standards, such as FibreChannel, Infiniband and PCIe, address specific applications for storage, compute and communication functions. Non-hierarchical (ideally) or flatter network architectures deliver the best performance for parallel systems. Switches serve to reduce contention by reconfiguration at a cost of port count, energy and possibly latency for the completed function. Transparent, broadcast networks (All-to-All) could take photonic carriers from a core to anywhere in the network at the expense of large receive buffers and scalability. Programming models for effective parallel processing do not exist, and fundamental changes at the data structure level may be required. A self-consistent solution of these challenges defines *Convergence*. The *Convergence* solution may be general or it may require a change to 'special purpose' architectures. In either event, *both local and global control of switches, data rate and local component sleep/shutdown with photonic links will be necessary.*

Packaging has a controlling influence of on architecture. System design has a 3.5 year design cycle, while packaging has traditionally had longer design cycles. The flattening of architecture with parallelism is limited in implementation by interfaces and physical port design. For architecture to venture into converged regimes, packaging must lead with power, I/O and density solutions. The TWG will be responsible for i) promoting a 'package-first' design philosophy and ii) raising the issue of packaging science and engineering to significance for academic research and for allocation of industry and government funding resources.

Implementing Architecture/Hardware/Software Convergence Designers at each functional plane operate at vastly different levels of abstraction. Architects apply established design rules to create functionality, while rarely considering components and software. Software designers prefer to work with standard APIs, and new programming models are rarely considered feasible or backward compatible. *In the absence of vertically integrated companies, both architecture and software design functions rear view operations with delays of several technology nodes for implementation of new component technology.* The Convergence process will be initially limited by i) establishment of shortened, mutually aware Design Cycles; ii) creation of a Learning Curve based on high volume manufacturing; iii) effective guidance to focus R&D efforts of the various industries and academic specialties to provide different parts of the solution.

Targets, Barriers, and Needs for the Possible; and Vision for the Impossible The path to scaling performance by increasing utilization of resources is driving virtualization. For system administration, virtualization is a new responsibility: support of function rather than of resources; and administrative costs now exceed the sum of hardware and physical plant as a result. Standardization of hardware, software and architecture is essential for the delivering the interoperability required for efficient virtualization. Preconfigured solutions for the data center architecture follows the history of the PC: initial customization of hardware and software, followed by commoditization by outsourced modularity. Outsourcing survives when competition

on component performance/cost can proceed for a fixed architecture solution. It remains to be seen whether the photonic components represent a disruptive force that cannot be currently commoditized, or whether, as today, photonics will be forced to retrofit into current architectures and compete with wires.

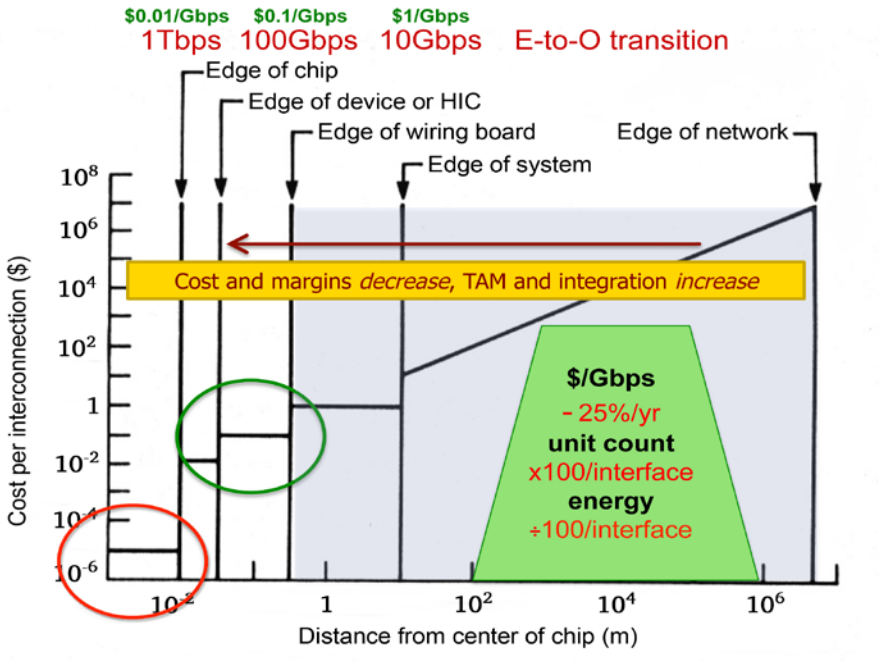

Figure 15. Scaling the Interconnection Hierarchy.

Performance, cost and business models for scaling the interconnection hierarchy. As single channel data rates increase to 1Tb/s, photonic signal transport will enter to package. The number of photonic packages will be $>10^4$ x the number of photonic network connections, and cost/connection must decrease by a similar $>10^4$ x factor.

Threshold for optical signaling Photonic interconnects are dominant in telecommunication networks, and they have successfully penetrated both data center and HPC rack-to-rack interconnection. In general, the transition from electrical to photonic interconnection occurs at a single-channel bandwidth x distance product of 1-3 Tb/s•cm (BxD = 1-3 Tb/s•cm). In 2017 single-channel bandwidth (B) will cross 400Gb/s threshold for board-level distances of >10cm. Board-level optical interconnection will require high volume manufacturing solutions with minimal impact on system cost. Package-level, intra-module photonic interconnection for distances of >1cm are forecast for ~2020 and data rates of 1-3Tb/s. Photonic interconnect solutions can meet system requirements for power and bandwidth density, but they have not yet met the cost point for pervasive intra-system deployment. Silicon photonics is being universally adopted to establish a 'future proof' platform that can achieve 'learning curve' cost reduction with cumulative production.

Table 8. Timeline and performance criteria for deployment of photonic interconnection.

Time Frame	~2000	~2005	~2010	~2015	~2020	~2025
Interconnect	Rack	Chassis	Backplane	Board	Module	Chip
Reach	20-100m	2-4m	1-2 m	.01-1 m	1-10 cm	0.1-3cm
BW (Gb/s, Tb/s)	40-200 G	20-100 G	100-400 G	0.3-1T	1-4T	2-20T
BW Density (Gb/s/cm^2)	~100	~100-400	~400	~1250	>10000	>40000
Energy (pJ/bit)	1000 -> 200	400 -> 50	100 -> 25	25 -> 5	1 -> .1	.1 -> .01

CRITICAL INFRASTRUCTURE ISSUES

DESIGN FOR MANUFACTURING

The integrated photonics value proposition is now well established and being commercially deployed to meet the power efficiency and bandwidth density requirements of information systems. In addition, a variety of 'sensing' applications and solutions that benefit from a platform featuring arrays and circuits of replicable devices are reaching the 'Internet of Things' marketplace. The associated manufacturing infrastructure is sized appropriately for current TAMs (Total Addressable Markets), but it is woefully inadequate for supporting scaling performance increases and cost reductions to support revenue growth. Furthermore, the current infrastructure does not: i) adequately leverage 'CMOS' standardization, ii) support a platform capable cross-market applications, iii) high levels of integration and iv) electronic-photonic synergy among components and circuits.

The most important near term infrastructure concerns are: Design Tools; Training of Designers; and Manufacturing Technologies: Materials, Component Technology, Standards Development, Intellectual Property Protection, Security and Information Management, Roadmap Identification of Paradigm Shifts and Strategic Concerns.

Infrastructure, however, is an evolving base for operations that requires a coherent long term plan with broad stakeholder adoption. If no paradigm-changing technologies emerge in the next two decades, the evolution of the integrated manufacturing infrastructure will likely follow the timeline below.

- **2015-18** Existing proprietary, company-specific and standard designs, which fulfill existing applications, if at a high cost.
- **2018-20** Evolution of Standards based on an interim Hybrid Approach to Photonic Chip Packaging
- **2020-25** Heterogeneous silicon photonics solutions with advanced 3D Packaging
- **2025-35** Monolithic Integration with Single Chip or Complex 3D Chip Solutions and minimal outboard photonic interconnection at the System Level.

Industry-wide adoption of scalable platform(s) The grand challenge is manufacturing system integration. Materials, design, packaging and functionality will require common investment in solutions

that can be adopted across the industry with support of expertise in a growing supply chain. AIM Photonics Institute is well positioned to lead this process, both in the US and across the globe. Commercial cost points will be achieved with "good-enough photonics supported by extensive electronic intelligence" as the science of electronic-photonic synergy is created. Cumulative manufacturing volume will be pursued with platform tradeoffs that support cross-market applications.

Scaling Manufacturing Cost Yield must be a focus from the beginning. Design for Manufacturing will incorporate simplicity, integration, packaging and production volume at the system level. Line yield and die yield will determine known good die, photonic test, reliability and redundancy practice standards. Test is a major contributor to cost with no direct contribution to performance. Photonic test variation is often larger than manufacturing variation. A design for test strategy will likely include built-in self-test (BIST) that is actuated and measured electronically.

DESIGN AUTOMATION

Design Automation Seamless compatibility must be established among digital/analog CAD tools and design rules. Lumped element device and circuit models will supplant first principles (Maxwell's Equations) simulation to allow a wide range of designers to participate in the industry. The models should be parametric, including speed, voltage, heat, isolation and mixed signal values. Robust design should develop immunity to device/circuit/system variation. Optical impedance matching, linearity, bandwidth, noise, power, thermal management and process integration should be embedded in design rules for geometry and layout. The projected timeline for implementation is given below.

2020

- validated PDK models for active and passive photonic circuits
- models for hybrid ASIC-on-optical interposer
- compatibility with evolution of SM, DP, multilevel coding, ...
- *foundry infrastructure: IP licensing/indemnification*
- look-up database; licensing fees

2030

- validated PDK models for electronic-photonic circuits
- validated chip-level thermo-mechanical models
- validated package-level thermo-mechanical models
- *single electronic-photonic IC/package design platform*

PRIORITIZED RESEARCH NEEDS (> 5 YEAR RESULTS)

Light Source Integration The solutions for optical and electronic power regulation and distribution are the most likely sources for paradigm changing technologies. Electronic power distribution utilizes the majority of ball grid array (BGA) connections, because thin wires are poor media for transporting high currents. Models for disaggregated data centers are considering novel architectures comprised of *multi-λ optical power racks*, server racks and switch racks. Can photonics provide the solution for electrical power distribution as well as for signal carriers and transmission? Waveguide integrated germanium photodetectors can efficiently provide voltage and current at standard CMOS levels; and each detector can generate >30mW of power. An optical power supply architecture that provides both electrical power and signal I/O could best perform with regulated wall plug light sources that are seamlessly transported to the chip/package through lossless interfaces that flatten the interconnection hierarchy. Such a system level design would be ideal for scaling parallelism. The main roadblock is a solution for the fiber-chip/package/board interface.

Scaling bandwidth density Consider the12 fiber ribbon as the footprint standard for scalable performance. The options for a 400G transceiver include 4 fibers coded at 16 QAM; 4 fibers with WDM 4 lambdas at 25Gb/s; 4 fibers with WDM 2 lambdas at 50Gb/s. QAM coding burns DSP energy. High data rates burn driver and TIA energy. WDM today requires TEC control. Athermal WDM wold allow scaling optical channel count beyond CWDM. A system level interconnect protocol design paradigm would be desireable. Such a design model would evaluate power, latency, and hardware implementation to create an optimized solution.

PRIORITIZED DEVELOPMENT AND IMPLEMENTATION (< 5 YEAR RESULTS)

Design Automation Seamless compatibility must be established among digital/analog CAD tools and design rules. Lumped element device and circuit models will supplant first principles (Maxwell's Equations) simulation to allow a wide range of designers to participate in the industry. The models should be parametric, including speed, voltage, heat, isolation and mixed signal values. Robust design should develop immunity to device/circuit/system variation. Optical impedance matching, linearity, bandwidth, noise, power, thermal management and process integration should be embedded in design rules for geometry and layout. The projected timeline for implementation is given below.

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- validated chip-level thermo-mechanical models
- validated package-level thermo-mechanical models
- *single electronic-photonic IC/package design platform*

Multi-Project Wafer Assembly (MPWA) The MPW process should include tightly coordinated joint development projects that explore options and implement platform solutions.

2020

- Optical power supply solution
- High radix matrix switch solution: >64x64
- Distributed gain block solution
- I/O and Power distribution for 2.5D (electronic and photonic)
- SM-everywhere compatibility
- Athermalization and/or scalable tuning: filters, modulators, lasers

2030

- Pervasive gain blocks with standard devices
- I/O and Power distribution for 3D (electronic and photonic)

Inline Control and Test (ICT) Electronic and optical inspection and test must be low cost through high yield, throughput and utilization of the inspection/control system.

2020

Design for Test

- Limit test protocols using one approach for both hermetic and non-hermetic devices
- Reduce test cost with rapid optical probe methods or BIST electronic probes
- Reduce test with high yield

Wafer level inspection

- High throughput photonic test
- Known good die
- Reduce test capex

2030

Wafer level inspection

- Functional test
- BIST: built in self test

Reliability and Redundancy Failure modes must be known with modeled dependencies on processing, materials and use. Fault tolerant design with low component stress levels and redundancy is essential.

- Known failure modes
- Early warning, fault prediction
- Standard hermetic and thermal test under operation
- Fault tolerant design
- built-in self-test

MONOLITHIC INTEGRATION TWG MEMBERSHIP

- Lionel Kimerling, MIT
- Corentin Monmeyran, MIT
- Mark Webster, Cisco
- Luca Alloatti, MIT
- George Celler, SOITEC, retired
- Pieter Dumon, IMEC/Luceda
- Madeleine Glick, U Arizona
- Mark Beals, MIT
- Richard Grzybowski, MACOM
- Irene Sterian, Celestica
- Jeff Shainline, NIST
- Mark Wade, MIT
- Jurgen Michel, MIT
- Michael Watts, MIT
- Dirk Englund, MIT
- Anuradha Agarwal, MIT
- David Bishop, Boston University
- Kazumi Wada, U. Tokyo
- Paul Juodawlkis, MIT
- Andrew Pomerene, Sandia
- Shinji Matsuo, NTT
- Attila Szep, AFRL
- Michael Garner, ITRS
- Robert Blum, Oclaro/Intel
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- Philip Lippel, MIT
- Rob Stone, Broadcom
- John Bowers, UCSB
- Chris Weaver, MIT
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- Alan Benner, IBM
- Nicholas Ilyadis, Broadcom
- Haifeng Liu, Intel
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PACKAGING OF ELECTRONIC PHOTONIC SYSTEMS

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PACKAGING OF ELECTRONIC PHOTONIC SYSTEMS

EXECUTIVE SUMMARY

The global network requirements are changing with the rise of the internet of things (IoT) and the migration to the cloud of data, logic and applications. These changing requirements must be accommodated while maintaining the pace of progress in size, cost and power per function that we have enjoyed for the last 50 years based primarily on the benefits of Moore's Law scaling of CMOS electronics. The introduction of photonics into the transmission, processing and even the generation of data through optical based sensors is a key enabling factor for continued progress in these areas as we reach the limits of the physics and the benefits of Moore's Law scaling slow.

Packaging is a limiting factor in electronics today since it has not kept pace with Moore's Law in scaling. Today electronic packaging is more expensive than the package contents in many cases and it contributes substantially to increased power requirements and latency. The solution to these limiting factors is a work in process with innovations such as wafer level packaging (WLP), system in package (SiP) architecture, 3D integration and heterogeneous integration. The integration of photonics into these emerging electronic packaging solutions is a focus of this Chapter but continued innovation in other areas will be essential.

There will be many specific challenges in realizing the benefits of integrating photonics into the fabric of the global network and the components attached to it. The solutions, however, cannot come from just packaging photonic components. The co-packaging of electronics, photonics and plasmonics will be required to address these substantial new challenges to meet the expanding requirement for higher performance, higher reliability, increased security, lower latency and lower cost of the future.

There will be new device types, new materials, new package production processes and new equipment required to accomplish these objectives. Some of these required innovations we know today but many specifics that must be addressed over the next 15 years are not known. The objective of this roadmap chapter is to identify the challenges with sufficient lead time so they solutions can be identified and proven before they become roadblocks to the pace of progress for the industry.

INTRODUCTION

The difficult challenges for the global data network over the next 15 years will be reducing the size, cost, power requirement and latency while delivering greater bandwidth and increasing reliability and security. The primary enabling factor will be the development of low cost, high performance photonic integrated circuits. These developments will address many of the manufacturing costs associated with the mechanical assembly of components on a printed circuit board and maintaining the mechanical stability required for photonic circuits. Packaging has been a limiting factor in meeting these requirements and it must be a major contributor in defining solutions for the future. The essential functions that a package must be provided include:

1. Protection for the contents of the package from the use case environment
2. Delivery of power for operation of the package contents
3. Provide data paths meeting bandwidth and latency requirements of use case application(s)
4. Isolation of signals internally to avoid noise and cross talk
5. Thermal and stress management to meet requirements of the package contents
6. Do no harm such as adding to power requirements and latency due to the package

These essential functions must be provided with the smallest size and lowest cost possible. The focus of this Chapter is identification of the difficult challenges and the potential solutions for meeting these challenges well in advance so the challenges do not become "roadblocks" to continued progress. The primary integration technology for the potential solutions will be a complex, 3D System in Package (SiP) architecture.

In order to identify the difficult challenges we are using two application areas from the Product Emulator Groups (PEGs) that will drive critical future requirements to focus our work. The applications are:

DATA CENTER SERVERS

The data center servers will require a package for heterogeneous integration of memory, logic, power controllers and photonics in 3D-SiP architecture to meet applications requirements in a controlled environment. The solution must also provide for packaging of replacements for existing "top of rack" components. These solutions must include SiP based traffic analysis supporting data path switching decisions selecting between photonic and electronic data paths and between packet switching and circuit switching. This will be a necessary capability to enable the most efficient use of the network resources for each type of data traffic. The packaging requirements for the data center and high performance computing are similar but not identical. The chapter will address the similar requirements together and separately address the critical differences that must be taken into account.

1. **Photonics for the Internet of Things**
   The internet of things (IoT) will require a package for heterogeneous integration of sensors, RF components, memory and photonics in 3D-SiP architectures. This must enable a general purpose SiP IoT hub packaging for environments that may not be well controlled. This capability will include energy scavenging to power the IoT hub in many cases.

Packaging for both Emulator Group applications must support flexible high volume package architectures that can accommodate multiple designs in each application area. The objective is to provide custom functionality with standard package architecture enabling high manufacturing volume. This will be an essential element in the requirement to drive down cost using high volume manufacturing over the 15 year life of this roadmap.

In addition to these system level applications there will be innovation required in single chip packaging to address new photonic components. Both SiP and single chip packages will require new materials, new processes and new production equipment. However, the Roadmap will assume that we adapt the manufacturing technologies for both photonic components and SiP packages developed by the semiconductor industry for electronic packaging wherever possible. This will avoid unnecessary time and cost associated with developing manufacturing capability for photonic packaging and the sub-systems and systems where these packages will be used.

Packaging for photonics will utilize equipment, processes and materials from the silicon device packaging technology where it is practical but there are differences in the requirements for photonics and electronics. The notable added requirements for photonics include:

1. Greater mechanical precision associated with alignment of optical components
2. Low cost, high density, high reliability optical connections into and out of the package
3. Thermal management that can accurately maintain temperature in a narrow range
4. Si and InP active devices with potentially different operating temperature requirements in the same package.
5. Greater sensitivity to stress which can alter the placement accuracy and the optical characteristics of photonic circuits.

The requirements for a reduction in cost and power by more than 1,000 times over the life of this Roadmap while increasing performance and reducing both size and latency will be addressed primarily through innovation in packaging. The most effective way to address these requirements includes moving active and passive components as close together as possible. This can reduce both power and latency by minimizing electrical signal length to reduce power consumption and decreases product size. This will also result in reduced cost as we come down the learning curve with volume production as illustrated in figure 1.

As Photons reach the package unit volume expands rapidly driving down cost

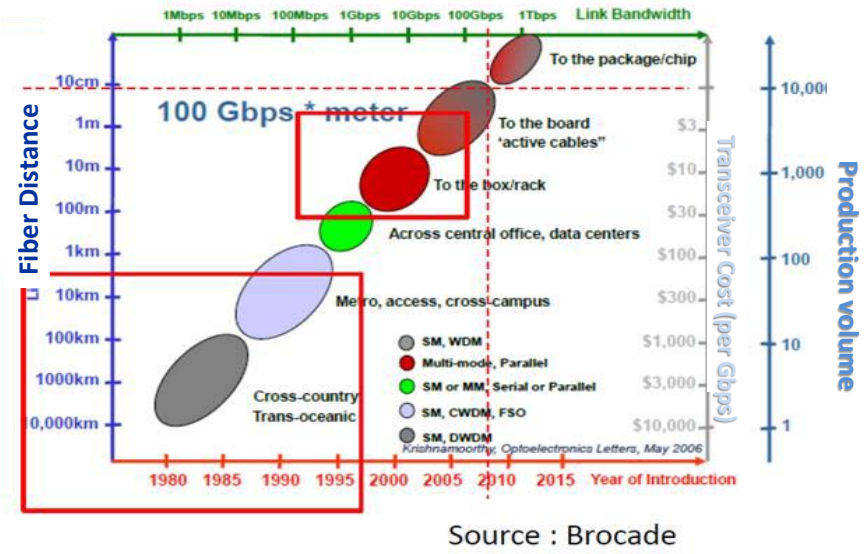


Figure 1: Moving Photons Closer to the Transistors Enables Cost Reduction

Supporting this cost reduction requires as much of the functionality as possible to be incorporated through monolithic integration as projected by the Monolithic Integration Chapter of this Roadmap.

Packaging technology has not kept pace with the progress in semiconductor devices. There was much more assembly in packaging ICs than in their production and there has been very little parallelism in the manufacturing of packages. The result has been packaging that often cost more than the contents of the package. Significant limitations in power, size, performance and latency were also due to packages rather than the active devices themselves. In order to avoid the cost and quality challenges of assembling many sub-millimeter components in a package we will rely upon wafer level packaging (WLP) as it is practiced today for electronics and future WLP approaches using reconstituted wafers and panel processing. The goal is to utilize the same parallelism in manufacturing for packaging that has driven semiconductor electronics cost reduction.

SITUATION ANALYSIS

The global internet traffic is projected to reach 2.0 zettabytes by 2019 from .7 zettabytes in 2014, a 23% CAGR. Two thirds of this traffic will originate from non-PC devices by 2019 with growth coming from TVs, tablets, smartphones and machine to machine communication. Each one of these growth sources has some important differences that will impact their packaging

requirements. Broadband speeds will more than double in the 5 year period from 2014 to 2019[1]. Despite the rapid growth of internet traffic more than 70% of data traffic in a data center will remain within that data center. The packaging solutions must accommodate this variety of differing bandwidth requirements, power requirements, size and weight requirements as well as security and reliability differences. The structure of the global network will change dramatically to meet the expanding requirements. The current "tree" architecture cannot meet this need with latency, power and cost that will dramatically exceed the market requirements. Innovation in packaging must be a major enabler of that change.

The emergence of the Internet of Things brings a host of requirements that are different from those of the Data Center, high performance computing and the high speed global network. Many of these "IoT nodes" will be located in areas that are difficult to access and therefore they will depend on wireless connectivity and energy scavenging to perform their function. The use case environment will often be very hostile relative to other applications for mechanical shock, temperature and humidity. These requirements are more challenging than for controlled environment use cases of the data center and high performance computing. This places significant requirements on the packaging as well as the package contents. The reliability requirement may be similar to the historical telecom network with targets for continuous operation of many years. The solutions to meeting these requirements must include intelligent redundancy in the package as well as continuous test while running and the ability to use the redundancy for dynamic self-repair.

These requirements pose many new packaging challenges but, at the same time, reduce the demand for delivering high power density, low latency and in some cases small size required by other applications.

PACKAGE/SYSTEM CO-DESIGN AND SIMULATION

The packaging solutions for photonic circuits must incorporate heterogeneous integration of different materials and different circuit fabric types. This adds unique challenges due to the differences in the coefficient of thermal expansion, mechanical properties and operating temperature requirements. In order to avoid the cost and time associated with building and characterizing physical prototypes followed by a redesign cycle these experiments and design verifications must be done in the computer. This means co-design and simulation of thermal, mechanical, electrical and, in some case, even chemical properties of the package. There are some CAD tools available today that partially address this need but there is nothing available today that is adequate. These tools must integrate across the boundaries from active and passive devices to full system level products as illustrated in figure 2.

[1] This material is from the Cisco web site and similar forecasts are available from other companies active in serving internet markets.

Tools for heterogeneous integration across boundaries of device, package, printed circuit board and product essential to migration to higher density (SoC, SiP, 2.5D, 3D, etc.) and time to market.

Electronics – Photonics – Plasmonics

This enables:

- ✓ Increased performance and bandwidth
- ✓ Decreasing latency, power, size, cost
- ✓ Reduced time to market

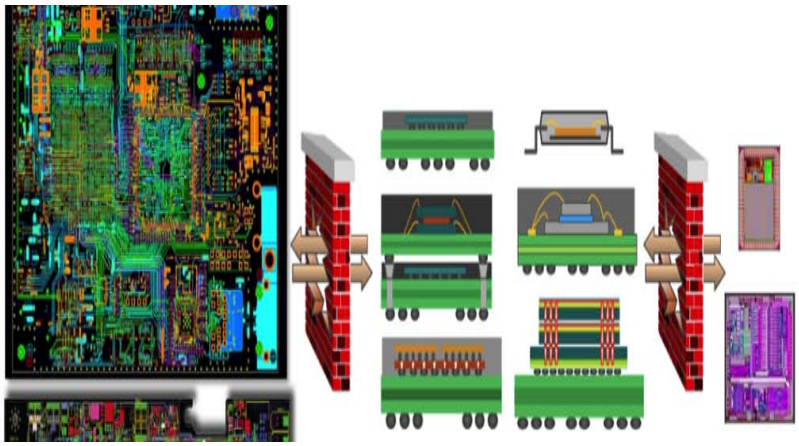


Figure 2: CAD Tools enabling design and simulation can prevent Challenges from becoming Roadblocks

These tools and photonic/electronic spice modeling are critical for the design of monolithic photonic integrated circuits as well as the packaging for those circuits. The incorporation of as many of the system features as possible into a monolithic photonic IC is the goal since it will address many of the difficult challenges such as cost, power, latency and performance. The accurate simulation of these monolithic photonic circuits will guide packaging by identifying requirements for:

1. Thermal management and temperature control
2. Stress management to reduce stresses imposed on the IC during the use case and thermal cycling
3. Component placement accuracy both for initial assembly and changes incurred through thermal cycling in the use case.

CAD tools available today may meet the needs of early development phases, when the design is focused at improving the functionality of single devices without paying attention to system characteristics. The SiP packaging design tools do not yet support the heterogeneous and 3D integration that will be required to do the development and design verification in the computer. This will be essential for the short product life cycles and short design times associated with the portable consumer products. This is a very complex problem since simulation requires detailed materials properties that are not available. As layers in a device or a package for that device become thinner the materials properties are increasingly determined by the interface rather than the bulk properties even when bulk properties are known.

This task is made more difficult as we incorporate new materials with properties that are not well known. Even if we know bulk properties, the mechanical and electrical properties of very thin layers are controlled more by the interfaces to dissimilar materials than by bulk properties. Understanding the controlling properties for new materials and very thin layers of traditional materials is a difficult challenge. If that challenge is not met we will have limited ability to optimize the design and construction of both the monolithic photonic circuits themselves and the packages that protect them without building and testing prototypes. This will not meet market requirements for cost or time to market.

The critical properties that must be known and taken into consideration in the design process are presented in Table 1 below.

Table 1: Critical Properties for Selected Materials

Material	Critical Properties
Electrical Conductors	Conductivity in 3 dimensions over processing and use case temperature ranges which are application dependent
	CTE in 3D at processing and use case temperature ranges
	Bonding/joining characteristics
	Conductivity in 3 dimensions over use case temperature range which is application dependent
Thermal conductors	CTE in 3D at processing and use case temperature ranges
	Electrical conductivity
	Modulus
	Fracture toughness
	Interfacial adhesion
Insulators	Breakdown field strength
	CTE in 3D at processing and use case temperature ranges
	Fracture toughness
	Modulus
	Dielectric constant
	Leakage current

Table 1 addresses some of the packaging materials and the critical properties for those materials. There are many other materials and materials properties that must be considered. These include:

1. Active materials (both optical and electronic)
2. Wave guide materials for optical signals
3. Die attach materials
4. Underfill materials
5. Solders
6. Mold compounds
7. Composite materials that may be electrical/thermal conductors or insulators

Properties for each of these materials for both the use case and processing temperatures must be known for the experiments and design verifications to be performed in the computer to save time to market and design cost. Further discussions of materials for specific functions are located in the relevant section of this Chapter.

HETEROGENEOUS INTEGRATION

Heterogeneous Integration for packaging refers to the integration of separately manufactured components into a higher level assembly (package) that in the aggregate provides enhanced functionality and improved operating characteristics. The components that will be assembled into the resulting complex 3D-SiPs may include:

1. Monolithic photonic ICs (incorporating photonics, electronics and plasmonics)
2. Other discrete optical components that are not integrated in the SiPh-ICs.
3. Si based logic and memory ICs
4. MEMS devices
5. Sensors (including a growing list of photonic sensors)
6. GaN power controller circuits
7. RF circuits
8. Compound (direct bandgap) semiconductor lasers
9. Optical interconnects to and from the outside world
10. Electrical interconnects to and from the outside world
11. Passive components (including integrated passive devices)
12. New devices and new materials that will enter the area over the life of this Roadmap.

Each of these components has its own packaging requirements that must be satisfied which results in a variety of complex packages. The package designs should use standard equipment, materials and processes where possible to reach high volume for each design. This will be key to driving down cost and improving reliability.

The monolithic photonic integrated circuits will include active electrical, optical and probably plasmonic devices that must coexist and, where possible, be manufactured with common processing technology. The use of a common process to build electrical logic, memory, power controllers and plasmonics will inevitably result in compromises to the process for each of the circuit types. The monolithic circuits using a single process is enticing but the compromises increase cost and power while reducing performance. Historically this has resulted in a disaggregated structure with multiple packages and costly assembly processes. We need the performance and cost of monolithic ICs and we also need the performance and cost of using the optimal material and process for each function. These two “needs” cannot be satisfied with today’s mainstream technologies. Recent developments in wafer level packaging offer the promise of approaching this “best of both worlds” scenario. We can build each circuit fabric type with the optimal material and process and assemble it at wafer level thereby retaining much of the parallelism in manufacturing required to control cost. The WLP technology also facilitates use of the third dimension; effectively reducing the physical distance between components which drives down power, latency and cost.

The increase in package substrate area for the SiP products and the historical processing temperatures that can range up to 400°C and the operating temperatures that are often limited to less than 100°C due to junction temperature limitations result in large stresses due to differential CTE between the package substrate and package contents. The result is warpage of the package substrate or components within the package. This issue will become more critical as we continue to decrease thickness of Si wafers, other package components and the layers of conductors and

dielectrics in the package interconnect to manufacture thinner products. This warpage results in assembly yield loss and may cause loss of mechanical stability required for photonic components. Even if we handle the warpage and assembly yield issues, the high processing temperature will result in substantial stresses built in at the lower use case temperatures. This is a yield and reliability limitation that must be addressed. It will become more important as the maximum junction temperature for silicon based logic and memory continues to drop to protect the sub-10ηm device geometries of the future.

This chapter will provide guidance to industry, academia and government identifying key technical challenges with sufficient lead time that they do not become roadblocks preventing the continued progress in data processing and communication that is essential to the future growth of the industry and the realization of the promise of continued positive impact on mankind. The approach is to identify the requirements for photonic packaging in the electronics industry through 2030, determine the difficult challenges that must be overcome to meet these requirements and, where possible, identify potential solutions.

BACKGROUND

The environment is rapidly changing and will require revolutionary changes after 50 years where the change was largely evolutionary. The major factors driving the need for change are:

- ✓ We are approaching the end of Moore's Law scaling
- ✓ The emergence of 2.5D and 3D integration techniques for packaging
- ✓ The emerging world of the internet of everything causing explosive growth in the need for connectivity
- ✓ Mobile devices like smart phones and tablets are growing rapidly in number and in data communications requirements driving explosive growth in the required capacity of the global communications network
- ✓ Migration of data, logic and applications to the cloud drives demand for reduction in latency while accommodating this network capacity growth.

Satisfying these emerging demands cannot be accomplished with the current electronics technology and they are driving new and different integration approaches. The requirements for power, latency, bandwidth/bandwidth density and cost can only be accomplished by revolutionary change in the global communications network, all the components in that network and everything attached to it. Ensuring the reliability of this "future network" in an environment where transistors wear out will also require innovation in how we design and test the network and its components.

The transistors in today's network account for less than 10% of total power, total latency and total cost. The interconnection of these transistors and other components in the IC, in the package, on the printed circuit board and at the system and global network level is where the future limitations in performance, power, latency and cost reside. Overcoming these limitations will require heterogeneous integration of different materials, different devices (logic, memory, sensors, RF, analog, etc.) and different technologies (electronics, photonics, plasmonics, MEMS. etc.). New materials, manufacturing equipment and processes will be required to accomplish this integration and overcome these limitations.

DIFFICULT CHALLENGES

The top level difficult challenges will be the reduction of power per function, cost per function and latency while continuing the improvements in performance, physical density, reliability and security. Historically scaling of transistors has been the primary contributor to meeting required system level improvements but this scaling is reaching its limits. Moving photonics closer to the transistors and heterogeneous integration can provide solutions compensating for the shortfall from the historical pace of progress we have enjoyed from scaling CMOS.

Packaging and test have found it difficult to scale their performance or cost per function to keep pace with transistors and many difficult challenges must be met to increase the rate of progress in packaging to maintain the historical pace of progress for data based industry. The key elements of the photonics packaging Roadmap are illustrated in figure 3.

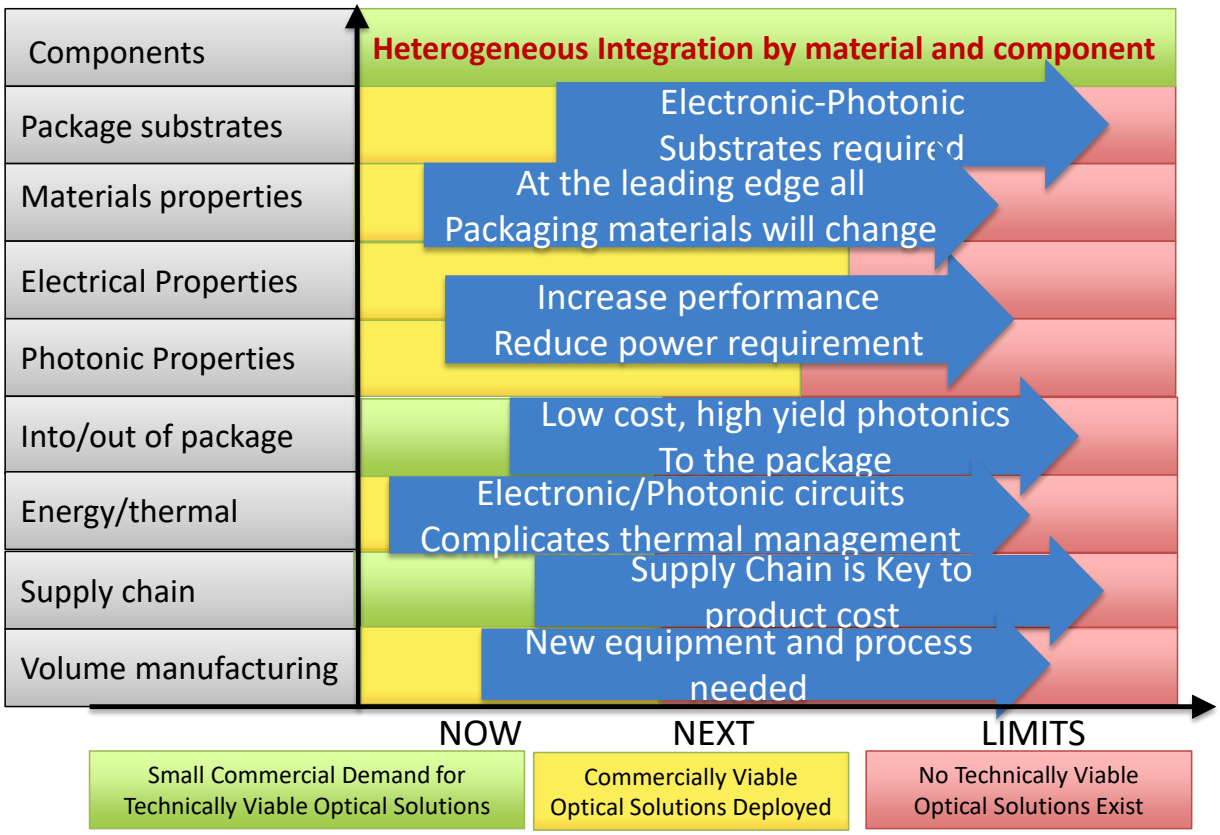


Figure 3: Photonic System Packaging Roadmap

The elements in yellow have known technical solution that do not meet the full requirements with cost and power being the primary reasons for shortfall. The elements in red currently have no know technical solution. Both of these categories pose difficult challenges.

An initial list of difficult packaging challenges for the two PEG emulators is presented in 3 categories; (1) On-chip interconnect, (2) Package assembly and (3) Test. These are analyzed to define the challenges that have the potential to be "show stoppers" for the application areas identified above.

ON-CHIP INTERCONNECT DIFFICULT CHALLENGES

The continued decrease in feature size, increase in transistor count and expansion into 3D structures are presenting many difficult challenges. While challenges in continuous scaling are not addressed here, the difficult challenges of interconnect technology in devices with 3D structures are listed. The challenges of incorporating photonics on a non-photonic chip versus the benefits of doing so are not yet clear. It is most likely that on-chip will be all electronic due to cost, switching speed and reducing interconnect length benefits associated with 3D-TSV architectures. The challenges addressed here assume that there is no optical interconnect on non-photonic chips. If innovation allows on-chip photonics (other than photonics chips) to be advantageous there will additional challenges not addressed here.

PACKAGE ASSEMBLY Difficult CHALLENGES

Package assembly is often the limiting factor in performance, size, latency, power and cost. Although much progress has been made with the introduction of new packaging architectures and processes through innovations in wafer level packaging and system in package for example, a significantly higher rate of progress is required. The complexity of the challenge is increasing due to unique demands of heterogeneous integration of electronic/photonic circuits. This includes integration of diverse materials and diverse circuit fabric types into a single SiP architecture and the use of the 3rd dimension. Many of the problems are the same as those addressed in the on-chip difficult challenges section. The additional difficult challenges associated with the package are listed below.

1. **TSV Formation [Cost: Design, Process, Materials]** Aspect ratio (via last) drives cost higher and the differential CTE causes local stress.

2. **TSV Operation [Reliability: Design, Materials]** "Cu pumping" out of the vias on thermal cycling. Thinner layers and reduced CTE differential will be needed.

3. **TSV Keep out area [Design, Materials, Process]** Circuit density and cost are impacted large keep out area due to differential CTE and increased stress sensitivity for photonic components. New materials and lower processing temperature are needed.

4. **Physical Density of Bandwidth [Size, Bandwidth: Design, Process, Materials]** Single mode WDM replacing multi-mode fiber/wave guides and integrated photonics chip supporting this capability on-package are needed.

5. **Low cost reliable optical connection to the package [Design, Materials equipment and Processes]** Process, materials and equipment for alignment/placement, bonding process for "wave guide soldering" to make cost effective and reliable connections to the package are needed.

6. **Low Cost Electronic/Photonic Package Substrate [Bandwidth, Waveguides, Design, Process, Materials]** Mechanical stability, thermal management, warpage control, photonic connections, electrical connections, integrated passive devices and other components will need to be accommodated. There are many candidates for package

substrate material that satisfy some of the requirements including glass, silicon, organic and ceramic but none of them satisfy all requirements. Silicon has the advantages of good CTE match, high electrical bandwidth, compatibility with optical wave guides and the wealth of experience, equipment and process technology from silicon IC fabrication that can be cost effectively reused. Glass has many electrical advantages but has poor thermal conductivity. Organics lack mechanical stability. Ceramics are expensive and also have thermal management limitations. It is likely that more than one of these substrates will be used for different applications.

7. **Thinned Wafers/Die at Low Cost [Design, Equipment, Materials, Process]** Today thinned die are typically processed to 50µ thickness and at that thickness will be warped to a level that they cannot be stacked without a method for maintaining flatness. Low cost residue adhesive and equipment to use it effectively in the thinning process will be required. Wafers in production will be thinned to 20µ thickness and lower during the life of this Roadmap. Techniques that work are known today but are not cost effective.

8. **3D Stacking [Cost, Process, Bonding, Thermal Management]** The processes used today are complex can be simplified with some expensive steps removed to lower cost and improve reliability. New materials and designs will be required for thermal management. Low temperature processing will be required.

9. **Stacking Heterogeneous Components [Design, materials, process]** There may be applications where the lowest cost and highest performance will require stacking of Si circuits and compound semiconductor circuits in the same stack. Differences in stress sensitivity and mechanical/thermal properties. New designs and materials will be needed.

10. **Noise and Cross Talk in SiP [Design, Process, Materials]** The SiP products will contain RF and other components that have low energy signals and logic that can draw high currents and impact the delivered power. Similarly as we reduce the physical separation of components in 3 dimensions cross talk can prevent proper operation. Some of these problems will become increasingly difficult as we reduce operating voltage due to both smaller geometries and the desire to reduce CV^2 energy requirements of the package. Designs that use optical signals where practical and shielding where optics is not practical will be required. New materials and processes will be required to manufacture these elements at low cost.

PACKAGE TEST DIFFICULT CHALLENGES

1. **Known Good Die [Design, Test Contacts, Materials, Process, Equipment]** The packaging of multiple die in the same package has relied upon known good die to ensure yield after assembly. This will not ensure reliability when transistors wear out and VLSI ICs today do not produce known good die. When there are billions of transistors per IC and the geometries are measured in nano-meters all die will have some defects. Intelligently designed redundancy can ensure a high yield of functioning die as they have in memory circuits for years. The concepts and implementation of testing to ensure

functioning die for logic is still a work in process. Contactless methods for test point access are being investigated but are not yet practical.

2. **Testing Silicon Photonics Chips at Wafer/Panel Level [Design, Equipment, Materials]** Low cost production of Si Photonics will require manufacturing and testing of packages with a high degree of parallelism. Wafer level packaging will require testing at wafer level to maintain cost. The design of low cost test solutions for single mode WDM photonics will be required. These solutions will be dependent on the co-design of the Si photonics chip, the test point contact and the test equipment itself.

3. **Low Cost Optical Test Access [Design, Materials, Process]** The incorporation of WDM single mode photonic signals on a package will require the ability to test the connections after package assembly. New concepts are under consideration but a cost effective solution does not exist. There will be design, materials and process changes to provide solutions.

4. **3D Stacking [Design, Testing, Testing Access Process, Equipment]** Testing and test access will require new designs for test access of stacked components. New test equipment to cost effectively test logic, memory, analog component, RF and passive devices in a single package will be required.

5. **Test Contactors for Contact Pads Below 5 Microns Diameter [New Contact Methods, New Materials, Design]** The test contactors in use today for electronics damage the pads they contact. This problem will be exacerbated as test pads are driven to thinner metal and sub-micron geometries. New test methods, new contact methods and new access design will be required, all must be low cost.

6. **SiP Reliability [Design, Testing, Thermal Management]** The more difficult challenges are associated with testing in a world where transistors wear out. We will have no known good die, traditional test access points will not exist and thermal management when areal thermal density is increased by a multiple determined by the number of layers in a stack will all require solutions . Innovation in design, materials and test strategy will be required to meet these challenges. New processes and materials will be needed with built in self-test, continuous test while running, intelligent redundancy and dynamic self-repair will be part of the solution. New materials and modifications to equipment will be required.

7. **Ensuring System Reliability for Electronic/Photonic SiP based Systems [Design, Software, Fault Localization]** The potential for a single point fault to prevent operation of data communication and analysis systems does not meet market requirements. There are two paths to reduce this probability of a system level shut down due to a single point failure. One is the use of intelligent redundancy which is identified above. The second is a system capable of quickly obtaining the physical location of a fault during the product qualification process so that revisions can be made to the design to remove or reduce the weak points in the system. The design of such capability for individual integrated circuits has been explored for several years. Extending this capability to cover all components in

a complex 3D Heterogeneous SiP is a very large task but will become a requirement to contain the cost of excess redundancy in these systems.

8. **Enabling the Software Defined Networks with Real Time Testing [Design, Software]** The diverse needs of users connected to the global network for access to the cloud will require SDN capability. This will not be practical unless the network hardware and software are configured to enable SDNs. This enablement will require low latency switching to set up the network and test capability to ensure that it is functioning correctly when set up and reliable during operation. The test challenge will require test resources at various points in the network that involve SiP incorporating FPGA technology.

DIFFICULT PACKAGING CHALLENGES BY CIRCUIT FABRIC

1. **Logic:** Hot spot locations not predictable, high thermal density, high frequency, unpredictable work load, limited by data bandwidth and data bottle-necks. High bandwidth data access will require new solutions to physical density of bandwidth.

2. **Memory:** Thermal density depends on memory type and thermal density differences drive changes in package architecture and materials, thinned device fault models, test & redundancy repair techniques. Packaging must support low latency, high bandwidth large (>1Tb) memory in a hierarchical architecture in a single package and/or SiP). Memory will have multiple circuit fabric types for various applications and each will have differences in packaging challenges.

3. **MEMS:** There is a virtually unlimited set of requirements; hermetic, non-hermetic, variable functional density, plumbing, stress control, and cost effective test solutions.

4. **Photonics:** Extreme sensitivity to thermal changes, O to E and E to O, Optical signal connections, new materials, new assembly techniques, new alignment and test techniques

5. **Plasmonics:** Requirements are yet to be determined but they will be different from other circuit types

6. **Micro-fluidics:** Sealing, thermal management and flow control must be incorporated into the package.

Most if not all of these will require new materials, new processes and new equipment for package assembly and test to meet the 15 year Roadmap requirements for electronic/photonic systems.

DIFFICULT PACKAGING CHALLENGES BY MATERIAL

1. **Semiconductors:** Today the vast majority of semiconductor components are silicon based. In the future both organic and compound semiconductors will be used with a variety of thermal, mechanical and electrical properties; each with unique mechanical, thermal and electrical requirements. Photonics and power management ICs will incorporate compound semiconductors with different thermal and mechanical properties.

2. **Conductors:** Cu has replaced Au and Al in many applications but this is not good enough for future needs. Metal matrix composites and 2D ballistic conductors will be required. Inserting some of these new materials will require new assembly, contacting and joining techniques.

3. **Dielectrics:** New high k dielectrics and low k dielectrics will be required. Fracture toughness and interfacial adhesion will be the key parameters. Packaging must provide protection for these fragile materials.

4. **Molding compound:** Improved thermal conductivity, thinner layers and lower CTE are key requirements.

5. **Adhesives:** Die attach materials, flexible conductors, residue free materials needed do not exist today.

PACKAGE COMPONENTS AND MATERIALS

PACKAGE SUBSTRATES

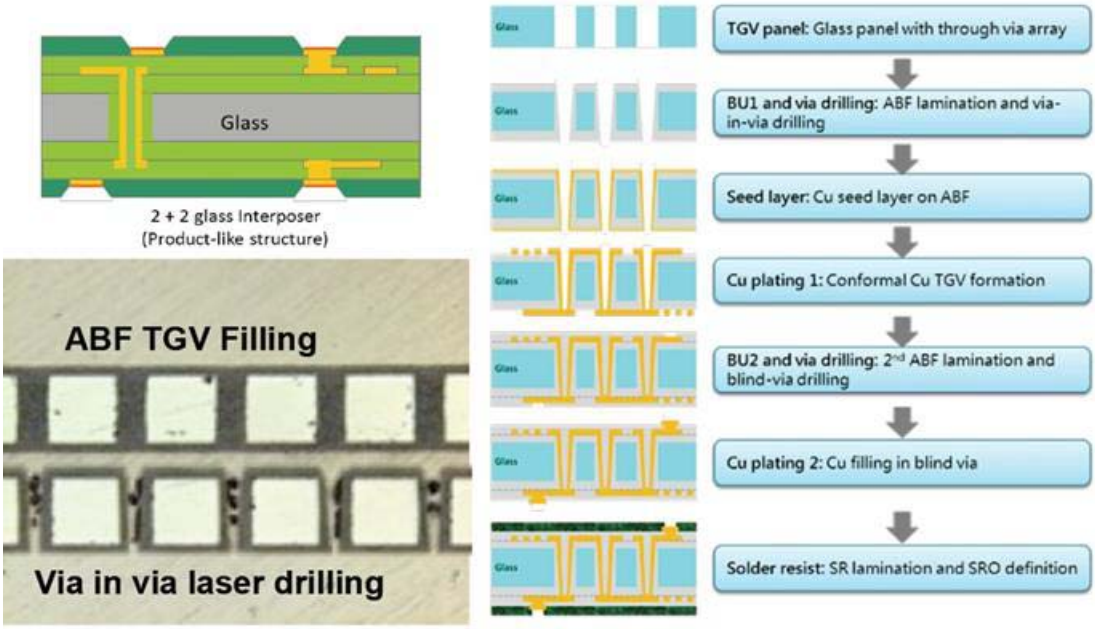
The dominate package substrate today uses organic laminate materials with limitations in mechanical stability, large CTE differential with silicon which limited wiring density. Today there are four different classes of material competing to be the package substrate of choice. They are:

1. **Organic laminates**
   Organics have the lowest cost but have limitations in lack of mechanical stability, limited thermal conductivity and a large differential CTE with semiconductors. It also accommodates embedded active and passive components much easier than any other package substrate material. Composites of organic laminates are continuing to make progress but do not meet future needs for photonic packaging. It is the solution of choice for single chip CMOS packages.

2. **Low temperature co-fired ceramics (LTCC)**
   This material has excellent mechanical stability, acceptable CTE match with semiconductors and good thermal conductivity but has limitations in wiring density, I/O pitch and cost. It is the solution of choice for harsh environments.

3. Glass

This material has advantages in high breakdown field strength, a true insulator which means essentially no leakage current and no variable capacitance. It does not match the bandwidth density of silicon and it has the worst thermal conductivity of candidate materials. There are several applications with low thermal density for which glass may eventually be the material of choice. There is a concerted effort to develop glass interposer technology for selected applications and it is likely that there will be high volume applications in the future where thermal density is not high. An example of the production flow for through glass vias (TGVs) is shown in figure 4 below.



Source: DC Hu, Semicon Taiwan

Figure 4: Glass TGV package substrate process flow

4. Silicon

Silicon has excellent CTE match, excellent mechanical stability and the best wiring density. Its limitation is in cost and, on a total cost per bandwidth basis, this limitation should be resolved as we come down the learning curve. It has better thermal conductivity than other substrate materials with the exception of some of the LTCC materials. It also has the limitations of a being a semiconductor which means variable capacitance and lower breakdown field strength. It is rapidly becoming the solution of choice for package with very high bandwidth requirements and it is the mainstay of the 2.5D integration currently in volume use for FPGAs.

The introduction of the silicon interposer has changed the package substrate for the most advanced packaging to silicon. This technology has been known for many years but was not adopted due to high cost. At the leading edge the interconnect density available using obsolete manufacturing equipment for 90-65ηm node ICs became cost effective for very high bandwidth interconnect. Silicon has the further advantage of embedding optical waveguide in the silicon substrate for heterogeneous integration of photonics, electronics

and plasmonics into a single package. There are 2 tables following that address the Silicon package substrates and the organic package substrates. There are no tables included for the other package substrate types since at present the other two seem to be limited to lower volume specialty packages. Table 2 below shows the critical parameters for the package substrate through 2030.

Table 2: Package Substrates for Heterogeneous Integration: High Performance, High End

Year of Production		*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2022*	*2024*	*2026*	*2028*	*2030*
Parameter	**unit**											
Package Type	-	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA
Interconnect Method	-	FC+TSV	FC+TSV	FC+TSV	FC+TSV	FC+TSV	FC+TSV	FC+TSV	FC+TSV	FC+TSV	FC+TSV	FC+TSV
Chip to Substrate Interconnect Land Pitch	µm	120	120	110	110	110	110	100	100	90	90	80
Max. Pin Counts	#	3600	4000	4000	5300	5300	6500	6500	7000	7000	7500	7500
Typical Pin Counts	#	3600	4000	4000	4500	4500	5300	6000	6000	6500	6500	6500
Min. External Cu I/O Pitch	mm	0.50	0.50	0.50	0.50	0.45	0.45	0.45	0.50	0.50	0.50	0.50
Min. External Cu I/O Pitch	mm	0.65	0.65	0.65	0.65	0.50	0.50	0.50	0.45	0.45	0.40	0.40
Typical Materials	-	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon
Typical Buildup Materials	-	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	ULK/SiO_2	ULK/SiO_4	ULK/SiO_6	ULK/SiO_8	ULK/SiO_{10}	ULK/SiO_{12}
Typical Interconnect Materials	-	Cu	Cu	Cu	Cu/Si	Cu/Si	Cu/Si	Cu/Si	Cu/Si	Cu/Si	Cu/Si	Cu/Si
Max. Layer Counts	#	4+2	4+2	4+2	4+2	4+2	4+2	6+2	6+2	6+2	6+2	6+2
Typical Finished Substrate Thickness	mm	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Core Material Tg	°C	1410	1410	1410	1410	1410	1410	1410	1410	1410	1410	1410
Core Material CTE (X-Y-Z)	ppm/°C	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
Core Material Dk@1GHz	-	12	12	12	12	12	12	12	12	12	12	12
Core Material Df@1GHz	-	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005
Core Materials Young's Modulus	Gpa	185	185	185	185	185	185	185	185	185	185	185
Core Material Water Absorption	%	0	0	0	0	0	0	0	0	0	0	0
Buildup/RDL Material Tg	°C	700	700	700	700	700	700	700	700	700	700	700
Buildup/RDL Material CTE (X-Y)	ppm/°C	3	3	3	3	3	3	3	3	3	3	3
Buildup/RDL Material CTE (Z)	ppm/°C	16	16	16	16	16	16	16	16	16	16	16
Buildup/RDL Material Dk@1GHz	-	2.0	2.0	2.0	2.0	2.0	1.8	1.8	1.6	1.6	1.6	1.6
Buildup/RDL Material Df@1GHz	-	0.003	0.003	0.003	0.003	0.003	0.001	0.001	0.001	0.001	0.001	0.001
Buildup/RDL Materials Young's Modulus	GPa	10	10	10	10	10	10	10	10	10	10	10
Buildup/RDL Material Water Absorption	%	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Min. Line width/Space	µm	5/5	5/5	3/3	3/3	1/1	1/1	1/1	1/1	1/1	1/1	1/1
Min. Conductor Thickness	µm	8	5	5	5	3	3	3	3	2	2	2
Min. Through Via Diameter	µm	100	80	80	70	70	70	60	60	55	50	50
Min. Through Via Land Diameter	µm	200	150	150	150	150	150	120	120	110	110	110
Min. Micro Via Diameter	µm	30	30	30	30	30	30	30	20	20	15	15
Typ. Micro Via Land Diameter	µm	60	60	60	60	60	60	55	55	50	50	50
Min. Through Via Pitch	µm	275	275	275	250	250	250	250	250	220	220	220

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

Notes for Table P1

1. After 2014, Silicon Interposer will introduce to High End Packager

2. After 2015, Core Materials will be changed to MEMS based cooling device which will use micro fluidic.

3. After 2017 silicon wave guides will be uses for optical signal interconnect

4. After 2019 ultra-low k dielectrics will be incorporated into the RDL build up

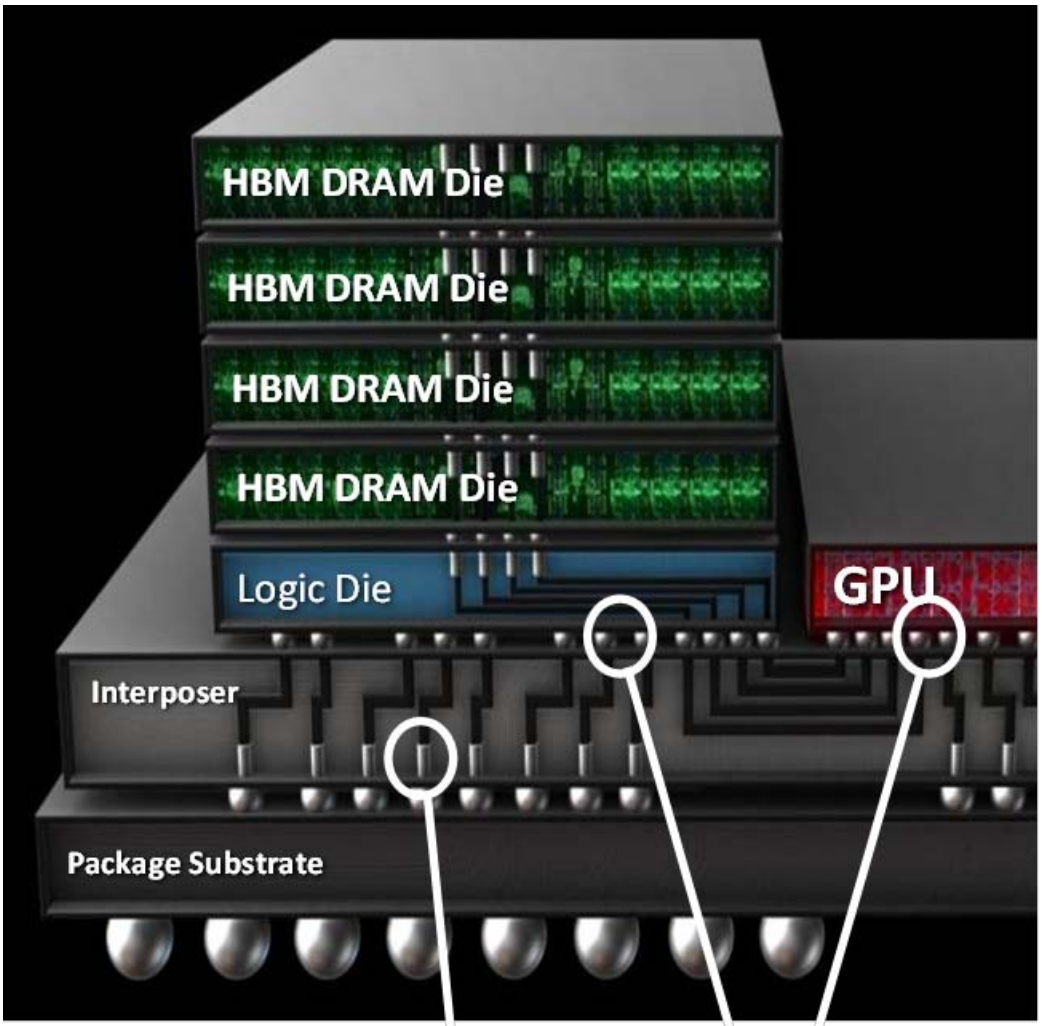
5. State of the art materials may not be compatible with cost requirements for volume production

6. Water absorption test is: JIS C6481

7. There are several parameters that do not change over the period covered by the Roadmap. They are:

Max. Body Size	*mm×mm*	*Typical Body Size*	*mm×mm*

In some cases, based on warpage considerations and/or minimum pitch on a system level printed circuit board where the package is to be mounted a combination of both a silicon substrate (interposer) and an organic package substrate are employed between the active devices, the silicon interposer may be mounted on a lower cost organic package substrate with a larger pad pitch. Figure 5 below illustrates this architecture which is in high volume production today.



Source: AMD

Figure 5: 3D-Sip Package using Silicon Interposer and Organic Package Substrate

The example above illustrates the use of a silicon interposer as a substrate for logic, memory and a graphics processor connected by µbumps to the interposer. The organic package substrate is joined to the interposer through silicon vias (TSVs) with solder balls. The entire image constitutes a ball grid array (BGA) package with large solder balls on the bottom for connection to a system level printed circuit board. This product is the Fiji graphics processor from AMD and the package is in high volume production today. It represents the state of the art for 3D SIP packaging in 2015.

The characteristics of this organic package substrate used for mounting the silicon interposer are listed in Table 3 below.

Table 3: Organic Package Substrates: For mounting Silicon Interposer and other SiP components for Heterogeneous Integration

Year of Production		*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2022*	*2024*	*2026*	*2028*	*2030*
Parameter	**unit**											
Chip to Substrate Interconnect Land Pitch	µm	120	120	110	110	110	110	100	100	90	90	80
Min. Finished Substrate Thickness	mm	1.1	1.1	0.8	0.8	0.8	0.8	0.6	0.6	0.5	0.5	0.5
Core Material Tg	°C	210	210	210	210	210	210	210	210	210	210	210
Core Material CTE (X-Y)	ppm/°C	8	8	8	8	8	8	8	8	8	8	8
Core Material CTE (Z)	ppm/°C	10	10	10	10	10	10	10	10	10	10	10
Core Material Dk@1GHz	-	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Core Material Df@1GHz	-	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007
Core Materials Young's Modulus	GPa	24	24	24	24	24	24	24	24	24	24	24
Core Material Water Absorption	%	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07
Buildup Material Tg	°C	210	210	210	210	210	210	210	210	210	210	210
Buildup Material CTE (X-Y)	ppm/°C	12	12	12	12	12	12	12	12	12	12	12
Buildup Material CTE (Z)	ppm/°C	40	40	40	40	40	40	40	40	40	40	40
Buildup Material Dk@1GHz	-	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
Buildup Material Df@1GHz	-	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Buildup Materials Young's Modulus	GPa	5	5	5	5	5	5	5	5	5	5	5
Buildup Material Water Absorption	%	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Min. Line width/Space	µm	10/10	8/8	8/8	5/5	5/5	3/3	2/2	1/1	1/1	1/1	1/3
Min. Conductor Thickness	µm	15	12	12	10	10	5	4	3	3	3	3
Min. Through Via Diameter	µm	80	70	70	70	70	70	60	60	55	50	50
Min. Through Via Land Diameter	µm	200	150	150	150	150	150	120	120	110	100	100
Min. Micro Via Diameter	µm	50	50	30	30	30	30	20	20	20	15	15
Min. Micron Via Land Diameter	µm	100	100	70	70	70	70	50	50	50	40	40
Min. Through Via Pitch	µm	275	275	275	250	250	250	250	250	250	220	220
Min. Solder Mask Openning	µm	60	50	50	50	50	40	30	30	25	20	20
Min. Solder Mask Openning Tolerance	µm	18	15	15	15	15	10	8	8	8	6	6

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

Notes for Table P2:Organic Package Substrates: For mounting Silicon Interposer and other SiP components for Heterogeneous Integration

1. The package type for this table is P-BGA

2. After 2020, thin core buildup will be adopted for cost performance substrates

3. The interconnect method for this package is flip chip

5. State of the art materials may not be compatible with cost requirements for volume production

6. Water absorption test is: JIS C6481

4. There are several parameters that do not change over the period covered by the Roadmap. They are:

Max. Body Size	*mm×mm*
Typical Body Size	*mm×mm*
Max. Pin Counts	*#*
Typical Pin Counts	*#*
Min. External I/O Pitch	*mm*
Typical External I/O Pitch	*mm*
Typical Core Materials	*-*
Typical Buildup Materials	*-*
Max. Layer Counts	*#*
Typeical Layer Count	*#*

The Roadmap assumes that there will be no need for significant changes in geometries for this category since the first level of I/O count reduction and pitch translation will take place on the silicon interposer.

REPLACEMENTS FOR THE CMOS SWITCH WILL BE INCORPORATED IN 3D-SIP PHOTONIC/ELECTRONIC PACKAGES

The range of devices and subsystems in 3D SiP with Heterogeneous Integration includes a wide variety of system components with varied packaging requirements. The variety will continue to expand over the life of this Roadmap as new devices and materials with improved characteristics for specific functions are introduced and the use of 3D-SiP architectures expand to maintain the pace of progress as Moore's Law scaling continues to slow.

Si Integrated Circuits have now been demonstrated with geometries in single digit nanometers. The materials, equipment and processes available have enabled transistors that are near the limit of the physics. This continued scaling has not delivered the cost, power and performance improvements enjoyed historical Moore's Law scaling due. The ultimate demise of further scaling is an economic question rather than a technology limitation. When the cost of delivering a unit of performance is greater as we scale to lower geometries then scaling will stop. Many believe we are at that point today. This is a driving force to replace the silicon CMOS switch and there are several candidate materials. The paragraphs below show a number of devices made with materials that are candidates to replace silicon.

By adding black phosphorous over silicon, researchers at the University of Minnesota were able to achieve the on-chip detection performance level of germanium-based optical circuits. This high-level of performance occurs because a layer of 2-D black phosphorous significantly increases the optical circuits' interaction with light due to its narrow but finite band gap.

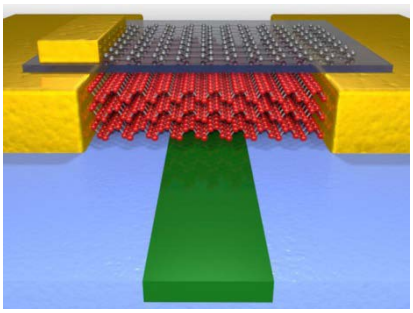


Figure 6: Black Phosphorous on silicon
Illustration from University of Minnesota College of Science and Engineering

Efforts continue to maintain the benefits of scaling. This example from IBM's T.J. Watson Research Center has reported scaling the 1.8 nanometer node and beyond to the angstrom level eventually using the same extreme-ultraviolet (EUV) lithography CMOS process technologies already in place. They identify the main issue for scaling being the contact rather that the ability to scale active area geometry.

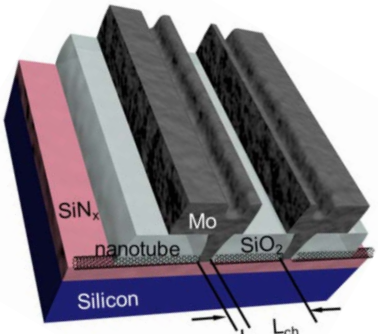


Figure 7: Nanotube transistor schematic with contact length <10nm.
Source: EE Times

There has been a growing list of 2 dimensional semiconductors with properties that are being investigated for replacing the CMOS switch. This is relevant for packaging since packaging requirements may be different for each one. As these options are developed we will need to update the Roadmap to incorporate those new devices and materials that are successful.

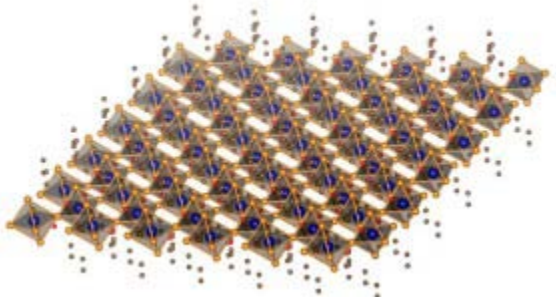


Figure 8: Structural illustration of a single layer of a 2D hybrid perovskite (C4H9NH3)2PbBr4)

Today the list includes:

1. Carbon nanotubes
2. Graphene
3. Black phosphorous
4. Molybdenum ditelluride
5. Molybdenum disulfide
6. 2D perovskites
7. Boron nitride

Only the carbon nanotube switch and the spin torque switch are in production today but work is underway on many more candidates for replacing the CMOS switch and we will have issues related to environmental requirements, thermal control, stress sensitivity, etc. that may require significant development if these new devices and materials are to be incorporated in the 3D-SiP package architectures of the future.

NEW PACKAGING MATERIALS WILL BE REQUIRED TO SATISFY MARKET DEMANDS

CONDUCTORS

The thermal and electrical conductors are both limiting factors in the achieving the improvements in power, performance, latency and cost. The state of the art of electrical interconnect today is copper with ultra-low κ dielectrics and for photonics it is active optical cables with multimode fibers. Both of these will have to change. The carbon based materials show great promise as shown in figure 9 below.

	Cu	CNT	GNR	
Max current density (A/cm^2)	**~10^6**	**> 1x10^8**	**> 1x10^8**	**x10^2**
Melting Point (K)	**1356**	**3800** (graphite)	**3800** (graphite)	
Tensile Strength (GPa)	**0.22**	**22.2**	**23.5**	**x10^2**
Thermal Conductivity (×10^3 W/m-K)	**0.385**	**1.75** *Hone, et al. Phys. Rev. B 1999*	**3 - 5** *Balandin, et al. Nano Let., 2008*	**x10**
Temp. Coefficient of Resistance (10^{-3} /K)	**4**	**< 1.1** *Kane, et al. Europhys. Lett.,1998*	**-1.47** *Shao et al. Appl Phys. Lett., 2008*	
Mean Free Path @ room-T (nm)	**40**	**> 1000** *McEuen, et al. Trans. Nano., 2002*	**~ 1000** *Bolotin, et al. Phys. Rev. Let. 2008*	**x25**

Figure 9: Carbon conductor properties look better than copper

Despite the advantages in current density and both electrical and thermal conductivity there are many questions that must be answered before either carbon nanotubes or graphene can be considered as practical inter connect materials. There process we use today for metal interconnects and heatsinks such as soldering, plating, lithographic patterning, TSVs, etc do not yet exist for these conductors.

Composite conductors are showing more promise. The results to date for composite copper show good progress in both conductivity and current capacity and the theoretical performance is about 3 times the progress today as shown in figure 10 below.

Composite Copper is in evaluation.

Current status:

Measurement	Conventional Copper	TeraCopper®
Resistivity (Ohm·cm)	**1.66×10^{-6}**	**1.26×10^{-6}**
Conductivity (S/m)	**6.02×10^{7}**	**7.94×10^{7}**
Increase in Conductivity	N/A	**32%**
Avg. Current Capacity(Amps/cm^2)	**3.88×10^{4}**	**5.57×10^{4}**
Increase in Current Capacity	N/A	**44%**

The first electrical performance improvement in copper since 1913 makes composite copper the most electrically conducting material known at room temperature.

Targets for improvement compared to conventional copper are:

- ✓ **100 % increase in electrical conductivity**
- ✓ **100% increase in thermal conductivity**
- ✓ **300% increase in tensile strength**

Source: NanoRidge

Figure 10: Composite Copper in Evaluation: Current Status

The more important improvement with composite copper is in the dramatic reduction in coefficient of thermal expansion. In the use case temperature range the CTE ranges between 4 and 5.5X10-6/°C vs 17 for OFHC copper. This has the promise of virtually elimination of stress and warpage due to differential thermal expansion which will be addressed in the package manufacturing processes section. The data on progress to date is shown in figure 11 below.

Measured Properties show:

- ✓ The strength of the Cu-SWCNT composite is more than twice that of pure copper
- ✓ Ductility is significantly lower.
- ✓ Coefficient of thermal expansion ranges between 4 to 5.5x10-6/°C vs 17x10-6/°C for pure Cu.

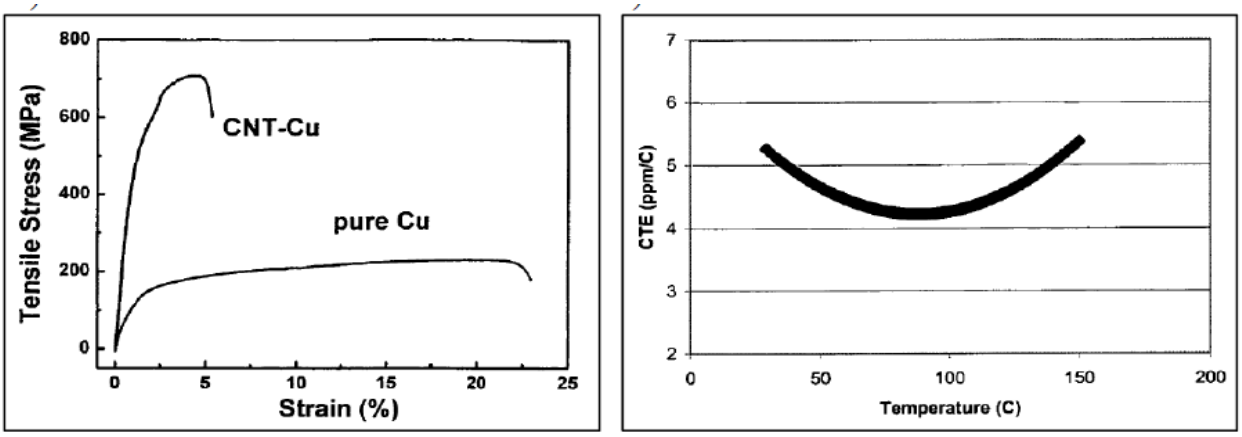


Figure 11: Coefficient of thermal expansion and tensile stress/strain comparison for OFHC and Composite copper.

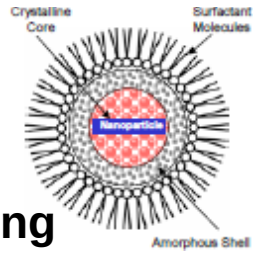
DIELECTRICS

Low κ dielectrics have been in use for several years with substantial efforts continuing to reduce the dielectric constant. Although there has been some success the practical dielectric constant still remains above 3 after processing for most of the candidate materials. There is a new generation of porous spin-on materials that have demonstrated dielectric constant below 2.0 but these materials are not yet fully qualified for production use.

JOINING MATERIALS

The joining/connecting materials in use today are primarily copper for interconnects either as wire bonds or copper pillars, soldering or direct interconnect bonding using either thermal compression or a low temperature DIP process (patented by Ziptronix). The high reflow temperatures for lead free solders result in joining the layers at ~250°C which is approximately 150°C above the maximum use case temperature which results in stress built in at the use case temperature. There are known solutions to this problem employed today. One is the use of nano-copper solder. This material was developed by Lockheed Martin and has been in use for space based applications for several years. The temperature of the melting of the solder is reduced by the high surface energy of very small particles so that joining can be accomplished as low as 150°C. Data for this material is illustrated in figure 12 below.

- ✓ **Package assembly at low temp (100C)**
- ✓ **Reflow solder to PCB <200C**
- ✓ **Consistent with Direct Interconnect Bonding**
- ✓ **Thermal/electrical conductivity 10-15X that of SAC**



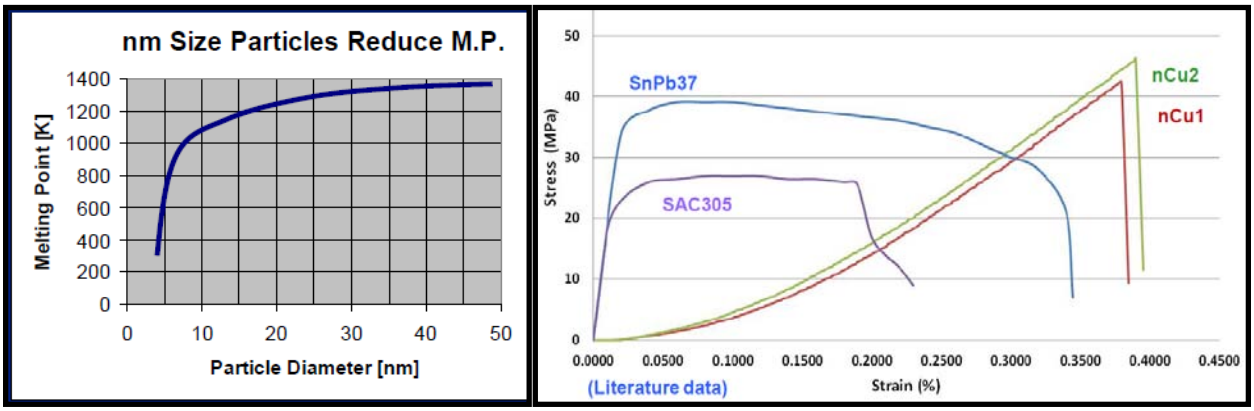


Figure 12: Properties of copper nano-solder, low processing temperature & improved conductivity

There are other developments taking place for improved thermal conductivity and mechanical properties for polymer composites that will also support continued progress for the electrical, thermal, optical and mechanical properties of advanced packaging that are not addressed in this Roadmap. The material above outlines in large part the current state of the art for electronics packaging that will be adopted for photonic/electronic SiP packages of the future.

PACKAGING PROCESSES

Cost reduction depends on reducing the amount of material used, reducing process steps, increasing the parallelism in the manufacturing process and improving yield. Each of these factors are addressed below.

REDUCING THE AMOUNT OF MATERIAL USED

As we move everything closer together the volume of material used is automatically reduced. Improving the conductivity of the interconnect material reduces the amount of conductor required. Thinner layers for all materials in the package from the substrate to the encapsulant reduce the amount of material used. New materials with improved electrical, mechanical and photonic properties will allow these reductions in layer thickness without compromising quality. The packaging industry has been doing this for several years and it is working but there is much more to be done.

REDUCING PROCESS STEPS

The current standard practice is to use underfill materials to improve the reliability of copper solder balls and pillars by improving the rigidity and strength of the electrical connection. The technology is available today to allow underfill to be removed thereby reducing the materials use and the number of steps in the process while improving reliability relative to the underfill process. The process flow is the following:

1. Use a direct interconnect bonding process from Ziptronix which results in bonding at temperatures as low as 100°C for both the copper and the surrounding insulator. This distributes the interfacial adhesion across a higher percentage of the surface.
2. Use composite copper to reduce the CTE differential between copper and the semiconductor material.
3. Assemble other layers in the package and attachment to the system printed circuit board with copper nano-solder.

The result is reduced material use, reduced number of process steps, joining at use case temperature of ~150°C to minimize stress and increasing the area of interfacial adhesion for improved reliability.

WAFER LEVEL PACKAGING AND PANEL PROCESSING

Wafer level packaging (WLP) has been defined as a technology in which all of the IC packaging process steps are performed at the wafer level. The original WLP definition required that all package IO terminals be continuously located within the chip outline (fan-in design) producing a true chip size package. This definition described a Wafer Level Chip Scale Package, or WLCSP, with the processing of a complete silicon wafer. From a systems perspective, under this definition, the limitation on WLP was how many I/O could be placed under the chip and still have a board design that can be routed.

Products coming to market today have more I/O than can be accommodated within the chip outline. The increased I/O density requires new packages known as “Fan-out” WLP (FOWLP). They are processed by placing individual sawn die into a polymer matrix that has the same form factor as the original silicon wafer. These “Reconstituted” artificial wafers are then processed through all of the same processes that are used for “real” silicon wafers, and finally sawn into separate packages. The die are spaced in the polymer matrix such that there is a perimeter of polymer surrounding each placed die. This area is used during redistribution (RDL) to “fan out” the RDL to an area larger than the original die.

This allows a standard WLP solder ball pitch to be used for die that are too small in area to allow this I/O pattern without “growing” the die to a larger size.

WLP technology includes:

1. Wafer level chip size packages (WLCSP)
2. Fan-out wafer level packages
3. Wafer capping
4. Thin film capping for MEMS devices

5. Wafer level packages with Through Silicon Vias (TSVs)
6. Wafer level packages with Integrated Passive Devices (IPD)
7. Wafer level substrates featuring fine traces and embedded integrated passives.

There are wafer to wafer stacking technologies that will support stacked die WLP for future products including heterogeneous integration of electronic ICs and photonic ICs (PICs). These technologies represent solutions to cost, power level, performance and size challenges for electronic/photonics products in the future.

WLCSP are mainly being used in portable consumer markets where small size, thickness, weight, and electrical performance are additional advantages to cost. Major trends include work for cost efficient rerouting with multi-layer RDL and improved design and simulation tools for WLP technologies.

With the introduction of TSVs, IPDs, Fan-out, and MEMS packaging technologies, WLP products can be used in a much broader range of applications, with higher I/O counts, and greater functional complexity. These packaging technologies open new opportunities for WLPs in the packaging field.

Figure 13 below shows a variety of FOWLP types currently in production.

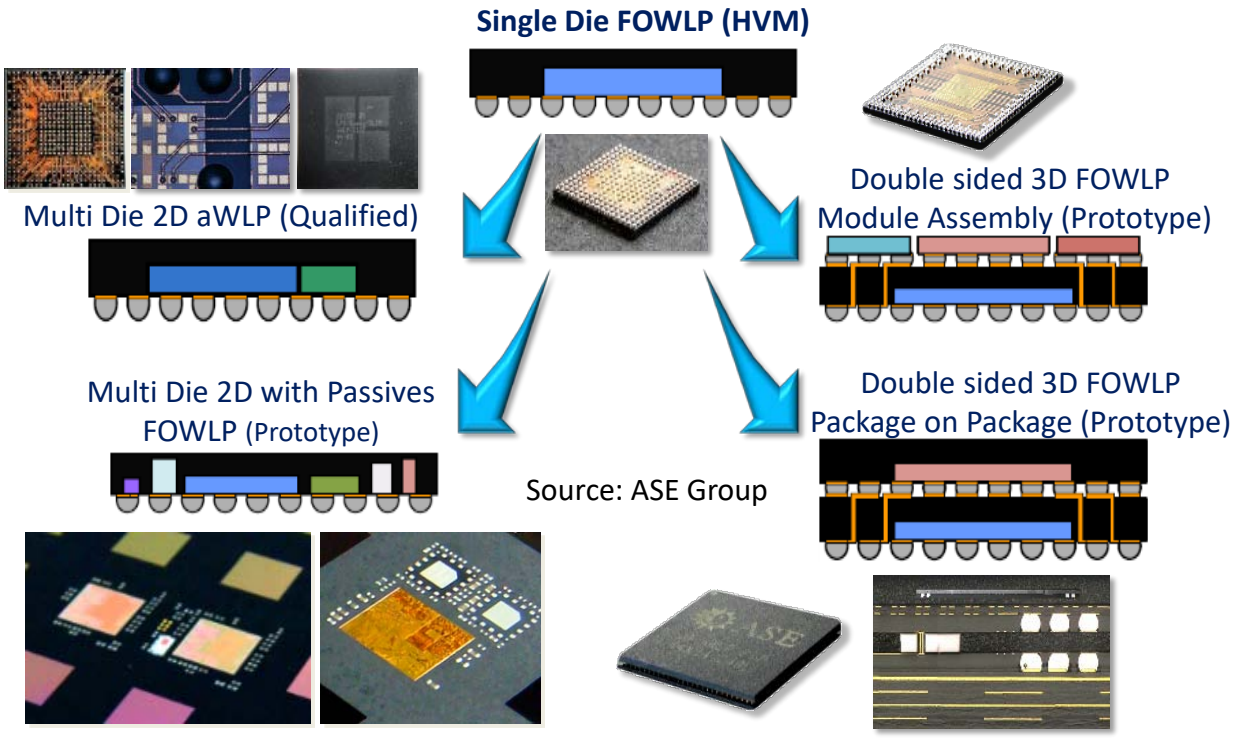
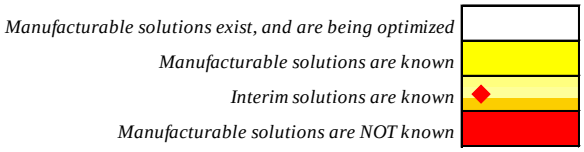


Figure 13: FOWLP in production qualification and production in 2015

Table 4: Critical Parameters for Wafer Level Packaging through 2030

Year of Production	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2022*	*2024*	*2026*	*2028*	*2030*
Cost per Area for Contract Assembly [1,2] (Cents/mm^2)											
a. Standard Logic and Analog/Linear – Low End	**0.11**	**0.1**	**0.1**	**0.09**	**0.09**	**0.08**	**0.07**	**0.06**	**0.06**	**0.05**	**0.04**
b. Standard Logic and Analog/Linear – Cost Performance	**0.23**	**0.22**	**0.21**	**0.2**	**0.19**	**0.18**	**0.16**	**0.14**	**0.14**	**0.13**	**0.12**
c. Standard logic, Analog and Photonic	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
d. Wafer Level Fanout	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**	**TBD**
Package size (mm^2) Including fan out and multi-die packages											
a. WLCSP- Memory	**20/250**	**20/250**	**20/250**	**20/250**	**20/250**	**20/250**	**20/250**	**20/250**	**20/250**	**20/250**	**20/250**
b. WLCSP-Standard Logic and Analog/Linear	**0.25/16**	**0.20/16**	**0.18/17**	**0.16/17**	**0.14/18**	**0.12/19**	**0.10/21**	**0.09/22**	**0.09/23**	**0.08/24**	**0.07/25**
c. WLCSP- Wireless: Bluetooth, FM, GPS, WIFI	**0.25/39**	**0.20/41**	**0.18/41**	**0.16/41**	**0.14/46**	**0.12/46**	**0.10/48**	**0.09/48**	**0.09/48**	**0.08/50**	**0.07/52**
d. Wafer level fanout	**2/144**	**2/144**	**1.8/156**	**1.8/156**	**1.6/169**	**1.6/169**	**1.5/182**	**1.4/196**	**1.4/210**	**1.4/212**	**1.3/215**
Number of RDL Layers per side											
a. All WLP	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	3	3	3
UBM Thickness (µm)											
a. Standard Logic and Analog/Linear (low power)	**1.5–50 µm**	**1.5–50 µm**	**1.5–50 µm**	**1.5–50 µm**	**1.5–50 µm**	**1.5–50 µm**	**1.5–50 µm**	**1.5–50 µm**	**1.5–50 µm**	**1.5–50 µm**	**1.5–50 µm**
b. Standard Logic and Analog/Linear (high power)	**1.1–50 µm**	**1.1–50 µm**	**1.1–50 µm**	**1.1–50 µm**	**1.1–50 µm**	**1.1–50 µm**	**1.1–50 µm**	**1.1–50 µm**	**1.1–50 µm**	**1.1–50 µm**	**1.1–50 µm**
RDL Conductor Thickness											
a. Standard Logic and Analog/Linear (low power)	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**
b. Standard Logic and Analog/Linear (high power)	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**	**2–15 µm**
Wafer Saw Street Width minimum(µm)											
a. All saw based singulation for WLP	**45 µm**	**45 µm**	**40 µm**	**40 µm**	**40 µm**	**35 µm**	**35 µm**	**33 µm**	**32 µm**	**31 µm**	**30 µm**
b. Advanced singulation (non saw techniques)	**20 µm**	**20 µm**	**20 µm**	**15 µm**	**15 µm**	**15 µm**	**15 µm**	**12 µm**	**12 µm**	**11 µm**	**10 µm**
Package Pincount Maximµm											
a. WLCSP	**240**	**256**	**256**	**256**	**289**	**289**	**300**	**300**	**320**	**350**	**350**
b. Fanout WLP	**550**	**600**	**650**	**650**	**650**	**700**	**700**	**730**	**730**	**750**	**750**
Package Ball Pitch Minimum (Note 6)											
a. All WLP	**250 µm**	**250 µm**	**250 µm**	**200 µm**	**200 µm**	**200 µm**	**200 µm**	**175 µm**	**175 µm**	**150 µm**	**150 µm**
Package Preformed Solderball Max Diameter for Min Ball Pitch (Note 6)											
All categories	**100 µm**	**100 µm**	**100 µm**	**75 µm**	**75 µm**	**75 µm**	**75 µm**	**65 µm**	**65 µm**	**55 µm**	**55 µm**
Package Minimum Backgrind Thickness (Note 6)											
a. WLCSP	**100 µm**	**100 µm**	**90 µm**	**90 µm**	**90 µm**	**90 µm**	**80 µm**	**80 µm**	**75 µm**	**75 µm**	**75 µm**
b. Fanout WLP	**200 µm**	**200 µm**	**190 µm**	**190 µm**	**180 µm**	**180 µm**	**175 µm**	**160 µm**	**150 µm**	**150 µm**	**150 µm**
Multiple Die Wafer Level CSP (Max. dies)											
a. Memory (Stacked)	**8**	**8**	**8**	**8**	**12**	**12**	**12**	**12**	**12**	**12**	**12**
b. Standard Logic and Analog/Linear (Stacked)	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**4**	**4**	**4**	**4**
c. Wireless: Bluetooth, FM, GPS, WIFI (Stacked)	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
d. Wafer level fanout (3D Stacked)	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
e. Wafer level fanout (2D Side by Side Die, each package)	**6**	**7**	**7**	**7**	**7**	**7**	**7**	**7**	**7**	**7**	**7**
f. Wafer level fanout (2D Side by Side Discrete Components, each package)	**10**	**12**	**14**	**16**	**16**	**16**	**16**	**16**	**16**	**16**	**16**
Stacked Die Wafer Level CSP Interconnect method (Through silicon vias, face to face, others)											
a. Memory	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**
b. Standard Logic and Analog/Linear	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**	**Mix of wire bond and flip chip stacked dies. Through Silicon Vias**
c. Wireless: Bluetooth, FM, GPS, WIFI	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**	**Through Silicon Vias**
Fanout WLP Technology	**Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules**	**Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules**	**Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules**	**Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules**	**Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules**	**Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules**	**Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules**	**Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules**	**Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules**	**Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules**	**Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules**

Notes for Table 4



Notes for Table P3

1. Entries defining the metallurgy that do not show changes over the next 15 years have been removed from the table. Any changes that might occur will be a result of the development of new materials.
2. the definition of WL-CSP is limited to 1.2 times die dimension or 1.4 times die area. Otherwise the fan out product would be just fan out WLP vs. CSP
3. Ball Mettallurgy is projected to be SAC for the next 15 years
3. UBM Metallurgy will have a number of variations depending on the company and the specific application. The metallurgy is not projected to change over the 15 years of the Roadmap.
4. RLD Metallurgy will have the same metallurgy for all devices and it is not forecast to change over the 15 years of the Roadmap
5. Type of WLP structure and metallurgy (bump, ball, column, solder, Cu, other). This metallurgy is not projected to change over the 15 years of the Roadmap. The metallurgy will be 2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar where ML= metal layer and P=polymer.
6. These parameters are driven by PCB manufacturing and cost issues and do not represent a limitation of the technology.

PANEL PROCESSING

The logical next step is to expand FOWLP to higher levels of parallelism through panel processing. Figure 14 below illustrates the path to increasing parallelism in packaging for cost reduction which has been underway for many years.

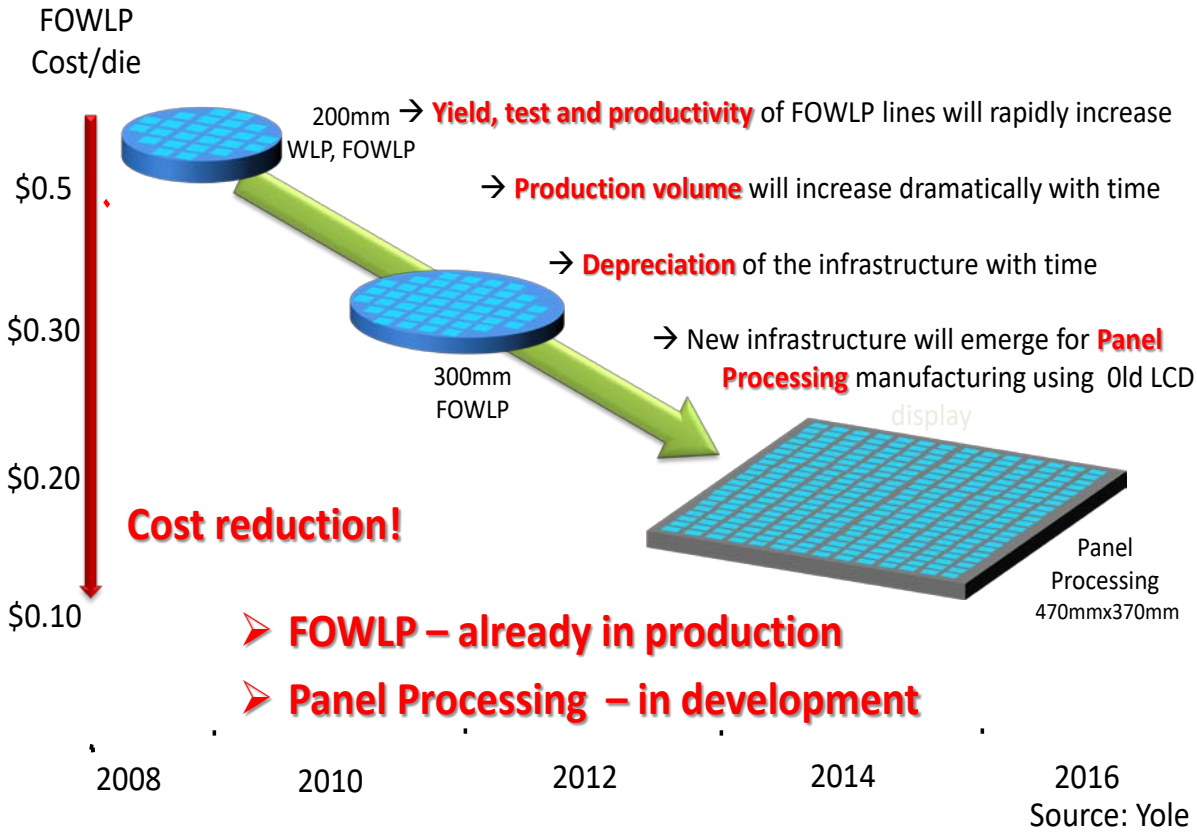


Figure 14: Cost reduction through increased parallelism in packaging

There are difficult challenges associated with implementation of panel processing while maintaining all the advantages of WLP outlined above. These challenges include:

1. Panel warpage (for Assembly accuracy & Manufacturability)
    a. Heterogeneous materials and non-symmetric structure causing bow
    b. New Polymer materials with matched CTE & modulus and low shrinkage needed
    c. Optimized layer sequence and design required

2. Accuracy/Resolution
    a. Improved optical recognition systems for placement equipment
    b. Die shift compensation
    c. Imaging with high depth of focus and high resolution
    d. Local alignment - LDI or scanner or stepper

3. Yield (and thus Cost)
    a. Suited materials and components
    b. Optimized processes

c. Production experience
d. Low k dielectrics for RDL to support high speed circuits
e. Low k with low loss are essential for RF performance

The use of Panel level processing is just being introduced into manufacturing and the typical process flow for is illustrated in Figure 15 below.

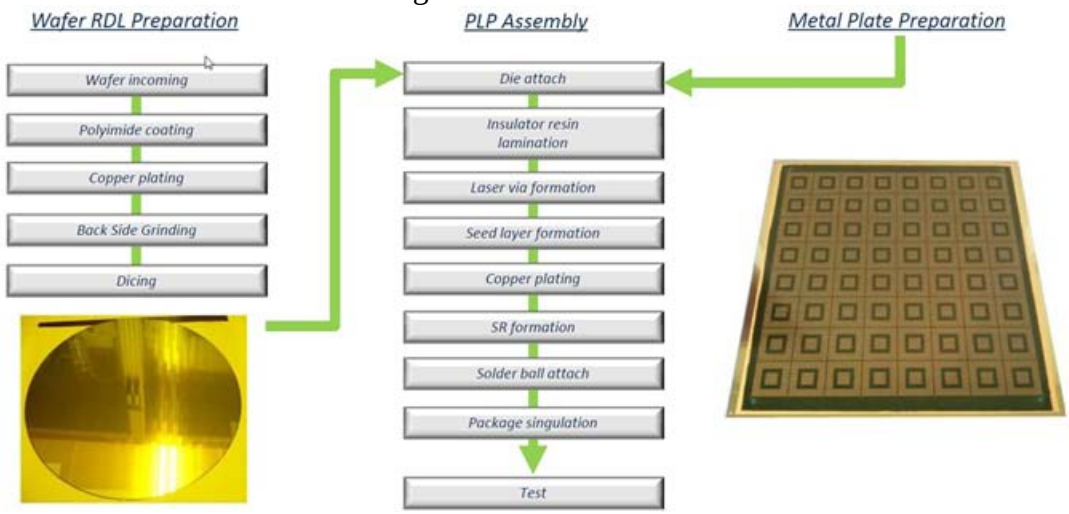


Figure 15: Panel level process for RF device (source: A Katsumata, Semicon Taiwan, 2015)

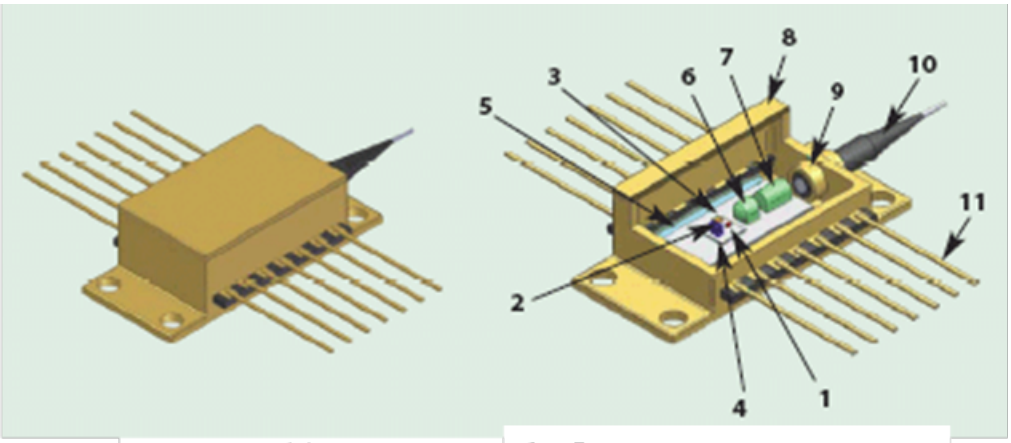
PACKAGING PHOTONIC DEVICES

There are a large number of devices that involve photons which share the common requirement of providing a photon path either into or out of the package or both. They include:

1. Light emitting diodes (LEDs)
2. Laser diodes
3. Plasmonic photon emitters
4. Photonic Integrated circuits (PICs)
5. MEMS optical switching devices
6. Camera modules
7. Optical modulators
8. Active optical cables
9. E to O and O to E converters
10. Optical sensors (photo diodes and other types)
11. WDM multiplexers and de-multiplexers

These devices have widely varying packaging requirements in power, photon access, alignment accuracy, stress management, thermal control etc. that can be handled addressed in a single component package but become much more challenging when they are integrated into a 3D-Heterogeneous SiP package.

The packaging of fiber optics initially was very simple consisting of a laser diode, a fiber and a photo diode. There was no motivation to integrate and the introduction of wavelength-division multiplexing (WDM) did little to change this since the transmit lasers were all on different line card. The typical laser diode packaging used in Telecom is shown in figure 16.



1. Laser chip
2. Monitor photodiode
3. Thermistor
4. Chip carrier
5. Thermoelectric
6. Lens
7. Optical isolator C
8. Component package
9. Window for light output
10. Fiber pigtail
11. Electrical leads

Figure 16: Butterfly laser package used in long haul telecom

This problem with this technology is evident from the figure. There are expensive components (gold), there is a high assembly parts count and it is very large in size. This approach is too expensive and too large to meet the requirements of low cost photonic systems.

The introduction of 100G Datacom has dramatically changed the situation since this requires multiple optical components in a small module which requires PIC integration. An example is shown in figure 17.

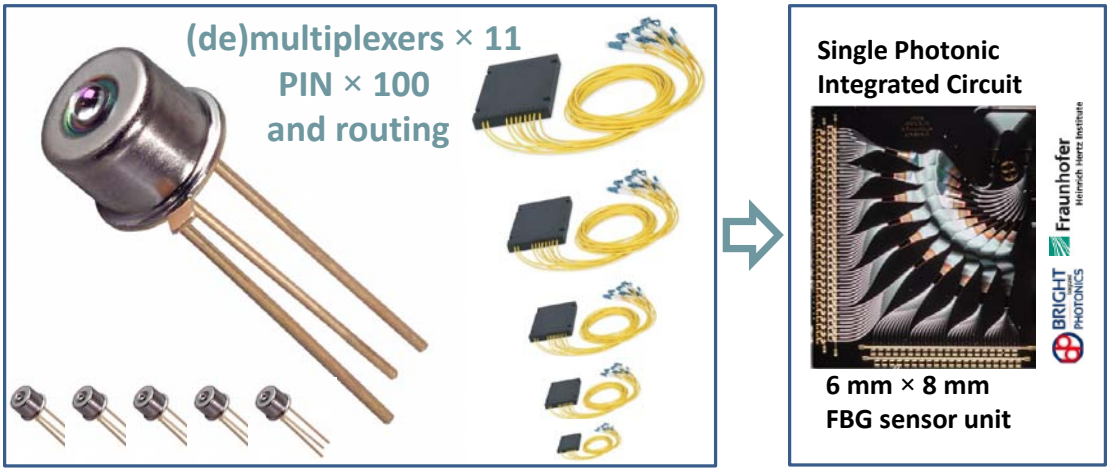


Figure 17: A Photonic Integrated Circuit combining multiple components (Source: Fraunhofer Institute)

This PIC enables smaller size, lower power and lower cost and it is available for use as a component of the 3D-Heterogeneous SiPs that will emerge during the lifetime of this Roadmap. Combining photonics and electronics in SiP products addresses the critical performance issues for the industry. They are summarized in figure 18.

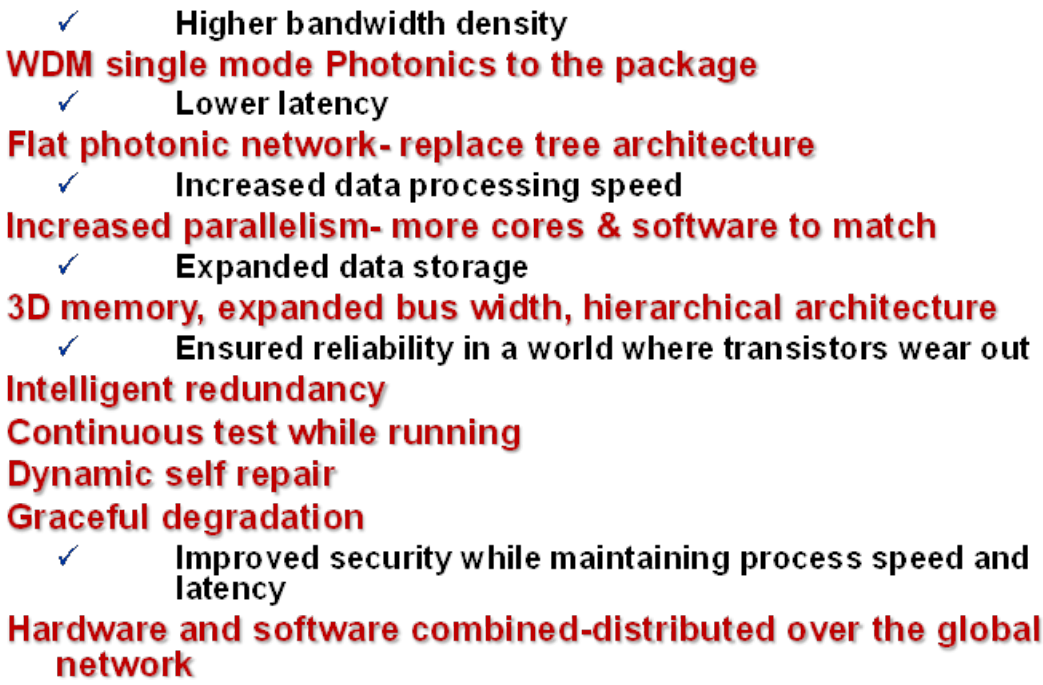
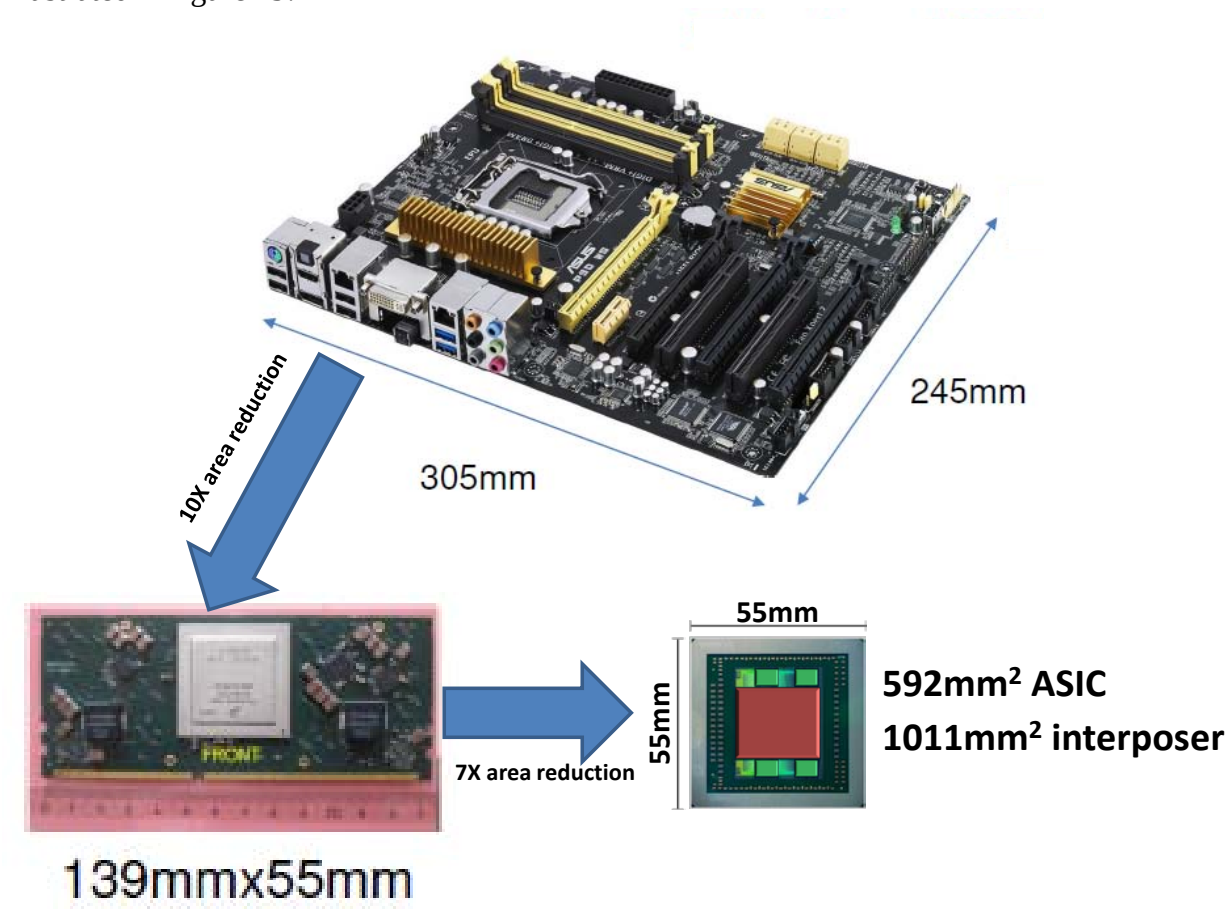


Figure 18: Potential Solutions to Support the Photonic/Electronic Roadmap of the Future

An example of the impact of combining new packaging architectures with state of the art components is illustrated in the work of Ronald Luijten of IBM in rethinking the server. Using conventional packaging techniques he was able to produce a micro-server into a single board with all the components other than memory reducing board area by an order of magnitude and

volume by a greater number. The addition of 3D integration in an SiP architecture enables adding the required memory while reducing area by an additional factor 7 and further reducing the volume. The result is lower power, high bandwidth, smaller size, higher logic performance as illustrated in figure 19.



The migration from the current server to the 3D SiP µserver can reduce area by 70X and volume by an even greater amount. This results in lower power, higher performance and eventually lower cost as high volume allows investment in automation. The next logical step is to add a photonic layer to the package to further reduce power and latency.

The current state of the art for photon approaching the transistors is illustrated in figure 19 with optical engines on cards with optical interconnects to the outside world and electrical interconnects to the packages mounted on the card.

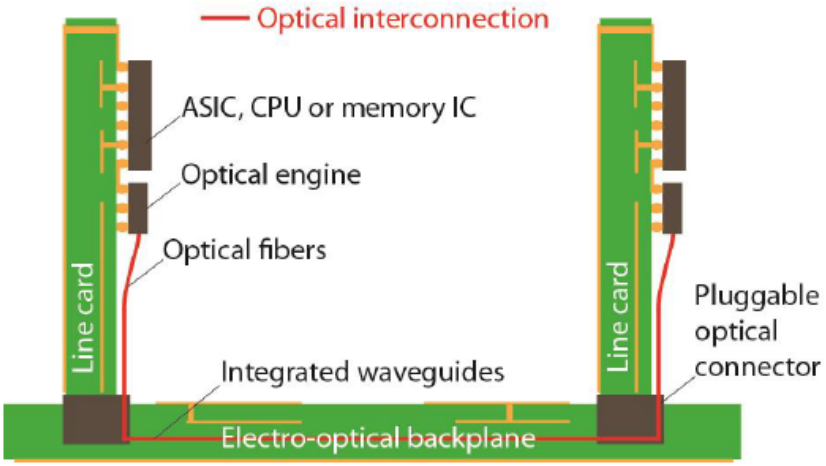


Figure 19: State of the Art for Photonics close to the transistors in 2015

The server or high performance computer system of the future will integrate PICs and with electronic ICs and mixed signal components for RF and power control. The future systems will have both optical and electrical I/O as illustrated in figure 20.

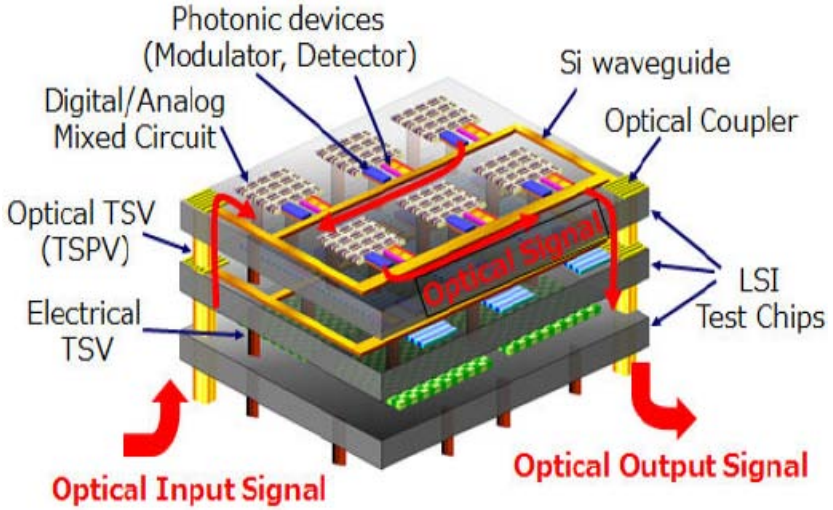


Figure 20: Future photonic/Electronic 3D-SiP with electro-optical package substrate.

SUMMARY

The inventory of components, materials, manufacturing processes and equipment needed to build the 3D-Heterogeneous SiP and the direction is defined by this Roadmap. A partial inventory of available components is illustrated in figure 21.

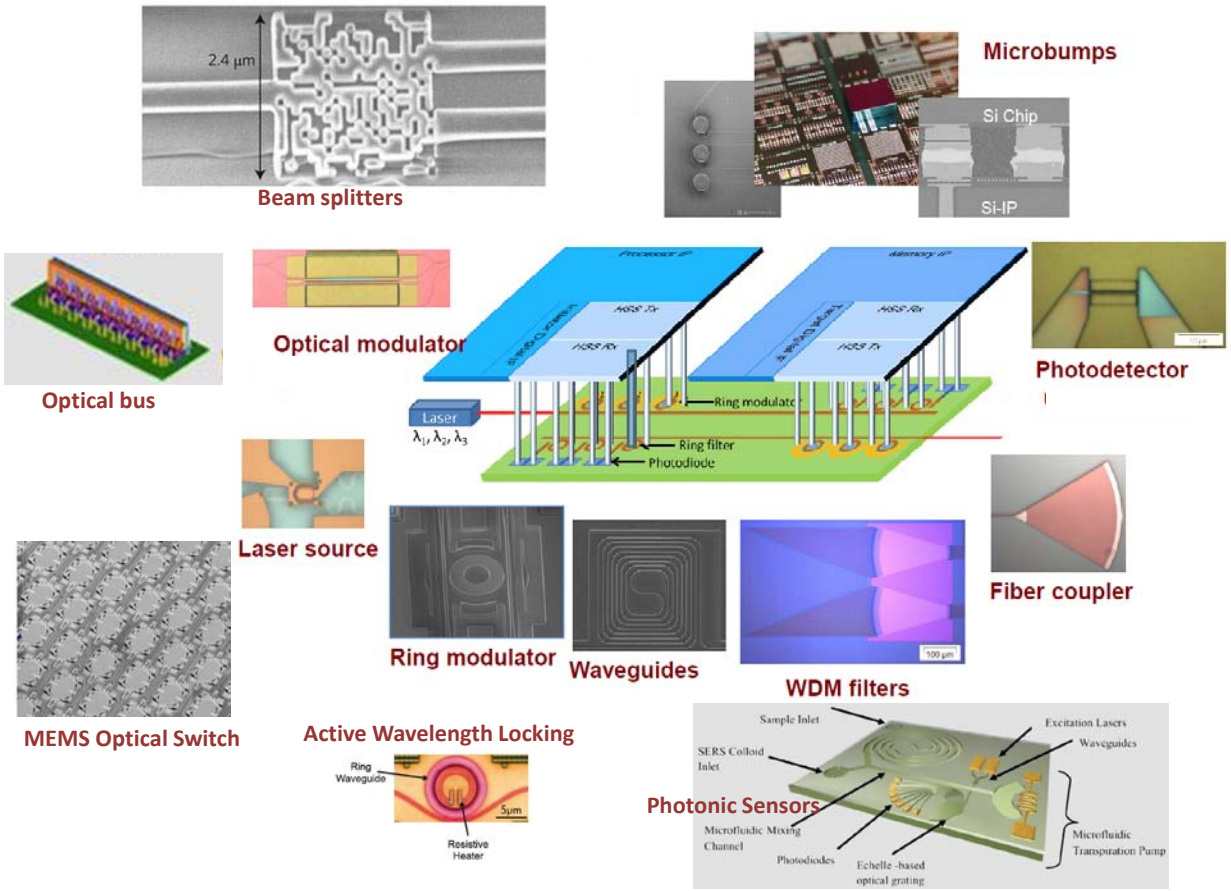


Figure 21: The inventory of proven photonic components is vast and rapidly expanding

The task of completing the Roadmap for packaging is to select from the attributes for photonic packaging listed in Table 5 below those that face difficult challenges and develop roadmap tables similar to P1-P3 which are based on electronic packaging and identify future the difficult challenges that must be overcome to deliver the improvements in cost, power, latency, size, reliability and security required by the 15 year forecast of this Roadmap.

Table 5: Attributes associated with Photonic/Electronic Packaging

3D integration in the package
Co-Design and simulation tools for all components: passive, RF, photonic, electronic, plasmonic, MEMS
Component attach for different materials and component types
Cross talk
Electrical connection into and out of the package
Electrical resistance/inductance/capacitance
Environmental compatibility
Hermeticity
Heterogeneous integration for diverse materials (different CTE, electrical, optical, mechanical properties)
High volume/parallel manufacturing processes
Incorporate changes over life of the roadmap in components and materials available
Low temperature assembly processes
Models for new composite materials
Photons into and out of the package
Physical density of components
Physical size
Reliability under stresses of the use case (thermal, mechanical shock, electrical, chemical)
Reliable power delivery with near threshold operation
Stress management
Test for complex SiP electronic-photonic products
Thermal management
Warpage (thinned components, package substrate)
Yield

KEY ATTRIBUTES ROADMAP

CRITICAL RESEARCH NEEDS

Critical Research and Development Needs
New materials with low temperature processing for packaging electronic/photonic circuits • Low CTE conductors with improved electrical conductivity • High κ dielectrics with high fracture toughness and interfacial adhesion • Low κ dielectrics with high fracture toughness and interfacial adhesion • Substrate materials CTE matched with components • Thermal conducting material for heat spreading and heat sinking much better than Cu • Encapsulant materials with low CTE and low modulus to avoid transmitting stress
New processes for joining stacked die at low temperature and minimum layer thickness
Zero residue adhesive to facilitate low cost high quality wafer thinning
Design & simulation tools for 3D heterogeneous electronic/photonic integration • Including materials properties for composites and very thin layers • Capable of design verification and optimization in the computer without need to fabricate prototypes • Co-design of thermal, electrical, optical and mechanical properties
Standardize platforms and parts

• Receiver • Transmitter • Transceiver • Multiple optical IO need to be standardized for each family
•
•
•
•

Gaps and Showstoppers

Recommendations on Potential Alternative Technologies
Explore the use of 3D printing to build a suitable substrate/platform upon which optical components can be placed, affixed and assembled in 6 dimensions that have smooth surfaces meaning to <0.1 microns RMS roughness.
Platforms for passive assembly that have well defined mechanical stops and associated methods to affix/weld/glue parts in place.
Methods utilizing capillary actions to “Pull” parts into place passively
Utilization of plasmons to minimize size and maximize functionality

A photonics design tool for advanced CMOS nodes
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INTERCONNECTION (CONNECTORS, CABLE ASSEMBLIES & PRINTED CIRCUITS)

Contents

INTERCONNECTION (CONNECTORS, CABLE ASSEMBLIES & PRINTED CIRCUITS)

EXECUTIVE SUMMARY

INTRODUCTION

Silicon Photonics technology (SiPh) is defined as photonic (lightwave) circuitry that employs low cost Si as a device and circuit platform and employs heterogeneous micro-packaging of various photonic chips and devices including GaAs, InP, and preferably Si micro-laser technology to drive low cost/high volume Computer/Datacom/Networking/Video Streaming applications. The compelling requirement for these technologies will be increasing circuit speed and bandwidth. These requirements are surfacing in high performance computing, data communication networks and data centers. Terabit speed will be necessary by the 2020s. OEMs recognize this paradigm shift from Cu to photonic circuitry. OEMs such as Cisco Systems, IBM and Intel are working on these technologies at the chip and system level. Intel has announced its Omni Path Interconnect Architecture which will provide a migration path between Cu and Fiber $\geq$ 40Gbps.

The Interconnect TWG encompasses the following Technologies:

- Existing and Fiber Optic Connectors (Focus on Single-Mode Fiber)
- Future EO Sockets and/or Interposers (EO Conversion from Metallic IC Package)
- Existing and Future FO Cables and Transceivers (AOCs, Board-Level Transceivers)
- Printed Circuit Boards (Organic FR4 Derivatives with Embedded Waveguides or Fibers)

Crosscutting Technologies covered in Packaging TWG:

- Interconnects within a SiPh SiP Package (Packaging TWG)
- Substrates employed in SiPh Multi-Chip IC Packaging (Packaging TWG)
- Direct Chip Attachment of SM FO Cables (SiPh Device TWG)
- Technologies Employed within the Semiconductor and IC Packaging Industries (Above)

Probable Future Technology Needs in Interconnect TWG:

#1: SiPh SM Fiber for High Speed and Bandwidth ($\geq$THz) Data Center, HPCC applications

#2: SiPh MM Fiber in Internet2, IoT, Industrial, Medical and DOD applications for noise-immune, environmentally rugged high speed and bandwidth applications ($\leq$GHz)

Probable Future Interconnect Product Designs (*and Challenges*):

- SM Fiber Optic Cable, PCB, IO Connectors (*Field Termination; Cost Targets*)
- InP/Si RX/TX: Board-Level Modules, Active Cables (*MM Designs in Production; SM Future*)
- Board Level Embedded Waveguide Connectors (*No Existing; Technology/Assembly/Cost*)
- EOPCB with embedded waveguide and interconnect technologies

SITUATION ANALYSIS - CONNECTORS

Electronic connectors are electro-mechanical and Electro-Optical connection devices. They basically connect circuit functions to wires, PC board traces or optical fiber to be precisely mated with minimum signal distortion. PC Boards are rigid and flexible organic substrates, mostly multilayer, that are the preferred circuit platform for most electronics.

- The connector market worldwide is in the range of $60B with an extremely diverse set of interconnect products and companies.
- Approximately 25% of connector volume is manufactured in the US, down from over 40% a decade ago. Connectors' supply chain is global, with different materials and processes scattered around the world, and with centers of excellence in Asia, Europe and North America.
- Of the major connector manufacturers, most are headquartered in the US, Europe and Japan. The global market for connectors is roughly 50% the top 10 and 50% all others which totals over 400 firms. Among the Top 10 connector companies (~ 2014 figures):

TE Connectivity: $13B
Amphenol: $4.6B
Molex $3.6B
Yazaki: $2.5B
FCI: $1.5B
JST: $1.5B
Hon Hai/Foxconn: $1.5B
Delphi Connection Systems: $1.5B
Hirose: $1.4B
JAE: $1.2B

US US/Switzerland Japan Taiwan France/Singapore Korea

FCI to be acquired by Amphenol

- Of the $60B in connector volume, *only 5% is in fiber optics via a small number of firms* who are mostly multinational companies with total revenues north of $500M. There are a few fiber optic specialists – particularly in Military/Aviation applications.
- Interconnect product developments and HVM capabilities necessary for a vibrant Silicon Photonics industry in the US will depend on these larger firms and a few smaller FO connector makers.
- Key to their involvement will be *leadership by OEMs to develop SiPh solutions, and commitments to pursue HVM of these new electro-optical solutions.*
- Among the SiPh applications that will require advanced fiber optic interconnects are the following:

• VCSEL heterogeneous active circuit modules converting metallic chip signals to photonics
• Monolithic Si Photonic SoC ICs for advanced, mid-2020s low cost lightwave systems
• Optical IC Sockets and Interposers
• Optical PCB Connectors
• Organic PCBs with embedded waveguides
• Input-Output FO Connectors
• EO Board-to-Board and Backplane Connectors
• MM & SM Fiber Optic Connectors in HVM
• Active Cable Assemblies
• Inter-System Cable Connectors

Table 1.1 Connector Levels of Packaging ***below is how one might define connector applications***

Level 0: On-Chip Interconnects (Al, Cu)	**Level 6:** Input/output Connections
Level 1: Chip to Package Interconnect (Wire Bonds, C_4, Cu Pillar)	**Level 7:** Inter-System Connectors, Cabling
Level 2: Package to Board Interconnect (Sockets)	**Level 8:** Local Telecom/Cable Plant
Level 3: PC Board Mid-Board/Board Edge Interconnects	**Level 9:** Long Haul Telecom/Datacom Plant
Level 4: Board to Board Interconnects	**Level 10:** Under Sea Cable Plant
Level 5: Chassis/Subsystem Level Interconnects	**Undefined:** Specialized Apps (e.g. IoT)

Purview of the Semiconductor Industry and PSMC Packaging TWG

MANUFACTURING EQUIPMENT AND PROCESSES

Fiber Optic Connector Equipment & Processes are varied depending on the design.

CONNECTORS, CABLE ASSEMBLIES AND TRANSCEIVERS:

- Stainless Steel, Ceramic and Plastic Ferrules and alignment structures are typically procured from outside: (UC Conec, Kinetic Systems, Thor Labs) and Japanese manufacturers
- Optical Fiber is procured from Corning Glass (Glass) and Mitsubishi (Plastic)
- Cables are procured from cable manufacturers with some produced in-house
- A main assembly process is Insert Molding (Precision Injection) with equipment procured from a number of mold equipment makers
- The typical assembly process is operator-assisted bench with precision alignment and optical inspection.
- The potential exists for automation via an in-line automated production line with insert molding technology.
- Fiber Optic connector manufacturing is mature technology; but potential exists for improvements in single-mode, turnkey cable assemblies and high volume automation: dependent on the staying power of a particular design.
- Not so with Active Cable Assemblies, which include Transceiver Modules containing InP transmitters and Si Receivers in a SiP assembly process. This process may gravitate to Si Optical Bench - or a more monolithic approach outside of the venue of connector manufacturing as Silicon Photonic technology progresses

CONNECTOR MATERIALS:

- There are ample suppliers of engineered plastic mold compounds, phosphor bronze and other metals used in connector manufacturing. The connector supply chain is global but mainly US and Japan. Dow Corning is active in this area.
- Optical Fiber comes mainly from Corning Glass, thus a very limited but stable supply chain. Expanded Beam lenses and others made from glass are available from a number of suppliers.

CONNECTOR QUALITY & RELIABILITY:

- There are quality & reliability challenges here, particularly in field assembly of single-mode cable connectors due to micro-level precision alignment and where particle contamination of the end face is possible. Endface cleaning and inspection are critical processes. This is addressed with factory terminated cable assemblies of varying lengths and fiber counts. It appears that factory termination is the best approach, particularly for HVM.

ENVIRONMENTAL TECHNOLOGY:

- There are no major issues here, although some may surface with future EU REACH derivatives in plastic mold compounds.

TEST & INSPECTION:

- Precision optical inspection is employed as well as testing fixed active and passive cable assemblies. Challenges will be on the test equipment side as data rates punch through 100Gbps toward Tb and Pb speeds over the next 20 years

SITUATION ANALYSIS-PRINTED CIRCUIT BOARDS

PRINTED CIRCUIT BOARD MANUFACTURING:

PCBs come in two varieties for mass-production of electronic circuits: Organic Rigid Multilayer PCBs; Flexible PCBs. Both can be “active” or “passive” and all are custom engineered for each application – unlike connectors, which have many standard designs. The closest a HVM PCB comes to that are the motherboards designed by Intel and others for the desktop PC.

Materials, Processes and other aspects of PCB manufacturing are covered in the 1100+ page IPC 2015 Roadmap, which was just released.

Several main issues with the PCB supply chain and materials are: i) historic pollution of PCB mfg. sites here in the US, which have been mainly cleared up through Superfund and other efforts and by changing PCB processes and chemicals This has also been a factor in chasing most HVM outside of the US, mainly to Asia; ii) the dirth of HVM left in NA due to transfer of outsourced OEM mfg. to EMS firms in Asia; iii) There are very few (<5) PCB manufacturers in NA exploring Optical PCB technology, none with actual products; iv) Flexible Polyimide and or Polyester PCB technology could, in many ways, be a key ingredient to a maturing OPCB technology, however, there are no known activities here to develop that technology, with the exception of silicone waveguide material developments at Dow-Corning with IBM Zurich. MFLEX would be a logical source; but they are focused on today’s electronic business and their large OEM customers.

Rigid PCB materials include a wide range of organic materials including Pre-impregnated epoxy-glass prepreg sheets, FR4+ Low-Loss Laminate materials, Copper Foil, additive Cu chemicals – and for the purposes of this effort, Silicone or other photonic materials to be applied as an outer or inner-layer optical substrate. PCB technology is the oldest electronic packaging technology in use today and has

evolved over 50 years to its current multi-faceted and global materials infrastructure. PCB processes include Prepreg, Imaging, Printing and Photo-Etching of Circuit Patterns, Lamination, Mechanical or Laser-Drilling of Vias and Micro-Via structures, and in some cases adding inner layer capacitor and resistor components. The ability to add layers of Silicone or other Polymer Waveguides should be relatively within existing technology; but connecting these optical traces to surface-level connectors will be a major challenge for HVM. Quite possibly, Taiwanese or Japanese manufacturers who support both PCB and IC Packaging Substrates may be in a better position to develop and commercialize – unless several US OEMs support an initiative with domestic PCB suppliers. Discrete cables are used today and this is not a bad solution because it provides the exceptional performance of optical glass fiber and existing FO connector technology. In the $65B Printed Circuit market, only one US company is in the top 10 of world PCB manufacturers and only 5 in the top 100, 4 after pending acquisitions (~ 2011figures):

	Unimicron: $2.5B		Hannstar Board: $1.2B
	Nippon Mektron: $2.41B	**#5**	TTM Technologies: $1.4B
	Ibiden: $2.1B		Semco: $1.4B
	Zhen Ding: $1.5B		Nanya PCB: $1.2B
	Tripod: $1.4B		Young Poong Group: $1.2B
#16	Multek: $0.9B	**#17**	Via Systems: $0.9B **(acquiring by TTM ⇧)**
#18	MFLEX: $0.8B (Flex)	**#41**	Sanmina-SCI: $0.4B

US US/Switzerland Japan Taiwan France/Singapore Korea

This creates a significant challenge to forward electro-optic capabilities in domestic PCB manufacturing. This may depend on a small number of firms – including supply chain technologists in waveguide technology. Organic laminated multilayer printed circuit boards are mostly rigid boards having etched copper foil to produce the surface mounting and interconnect structure, with OEM-specific circuit patterns from miniature devices to large electronic backplanes used in computer and datacom applications.

While there are a few development activities to enable optical traces in PCBs, current optical interconnect at the board level is near 100% done with cables and connectors.

The PCB market comprises over 1,000 firms worldwide, with organic PCB technology mature, with materials and knowhow in the public domain.

It is also an environmentally sensitive manufacturing industry, which has used corrosive chemicals, and has been beset by instances of Super Fund land pollution, which over the years has negatively affected production in the US.

Given that of the top 100 firms in this industry, only 5 are headquartered in the US, there are many smaller firms in the US that support wide-ranging applications from consumer to military. However, where HVM is involved, chances are the business has been moved to offshore facilities. If you look at

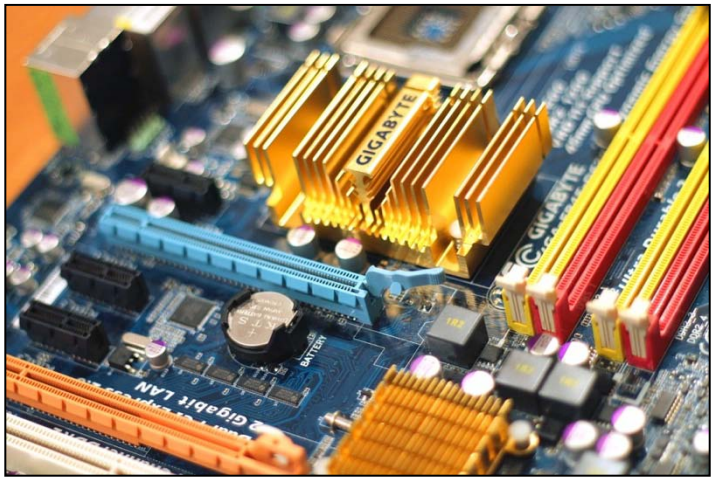
successful US firms, they will have facilities in Malaysia, Philippines, China and elsewhere in Asia, with a few in Eastern Europe.

Many are privately held, thus a miniscule percent of these PCB manufacturers have ventured into fiber optics, and where involved it is mostly Government-funded R&D and in a few specialized cases chip packaging applications. Firms in this industry are typically not highly funded or have sufficient margins to conduct a lot of research. Therefore, developments in fiber optics depend on OEM, Gov. and/or university research.

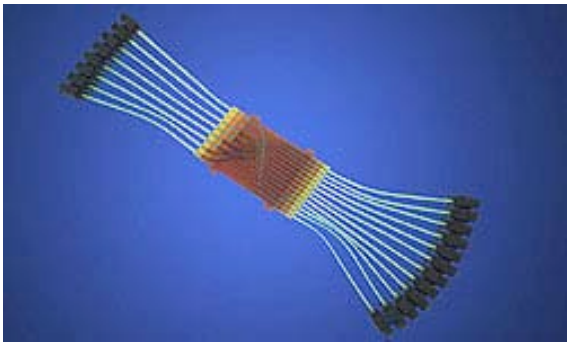
Conventional Multilayer PCB circuit platforms are exemplified by the PS/Server Motherboard which contains numerous components including CPUs, Chip Sets, Sockets, PCB and IO Connectors – all in Cu alloys. These boards, the backbone of a computer system, can support circuit speeds up to 10Gbps or more, depending on their physical size and componentry.

Replacing the circuits with photonic components and circuit traces is one of the requirement for a 40-100Gbps –to Terabit speeds in the future. It will require an OPCB with fly-over or embedded waveguides, optical transceiver modules, fiber optic connectors and cables supporting Silicon Photonic integrated circuitry and other photonic components.

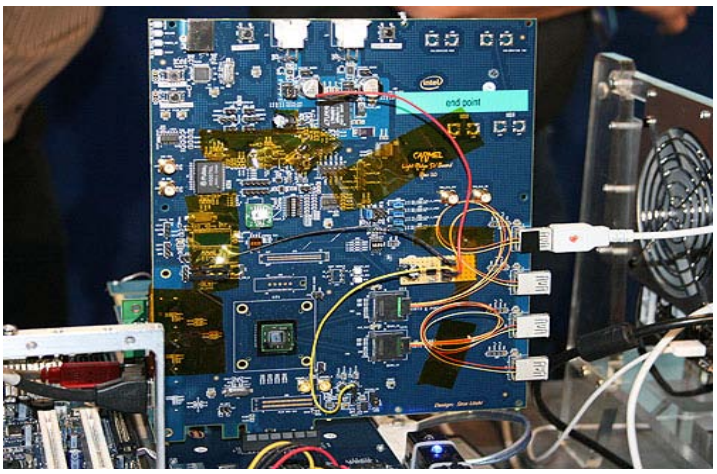
The challenges here are difficult but surmountable: (i) Si Photonic Integrated Circuits; (ii) A low cost organic Printed Circuit platform with fly-over FO cables as shown below, or ideally embedded waveguides connected to surface layer FO connectors with an optical via structure; (iii) board-level photonic components and transceivers where necessary to convert between photonic and copper signal traces; (iv) Input Output connectors and/or active cable assemblies; (v) aggressive cost targets based on 'cost/bit' and/or cost per component part. The latter may be more difficult than most technology challenges unless volume (100,000s to millions can be achieved.



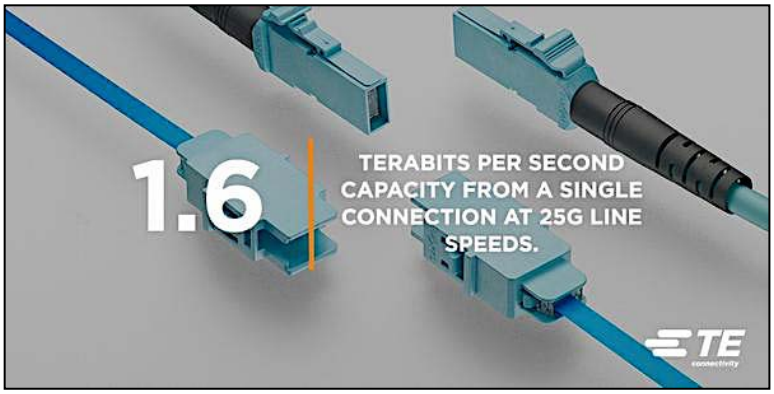
Gigabyte Motherboard



Molex Flex-Plane Circuitry



Intel Light-Peak Test Board (hardwarezone.com

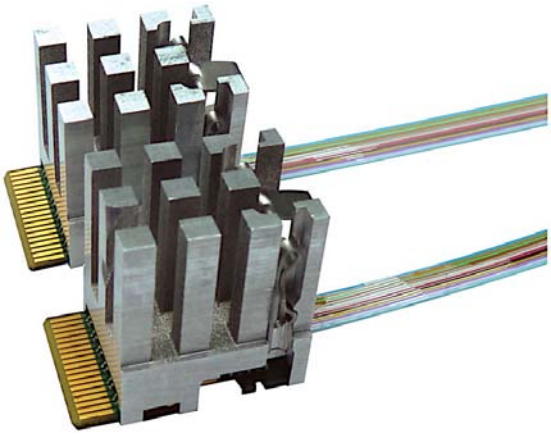


TE Connectivity MXC Connector up to 64 fibers/ferrule – YouTube:

"TE Connectivity: OFC 2015: MXC and MTP Comparison"

TE Cool Bit Mid-Board Optical Engine: 25Bbps/Channel – YouTube:

"TE Connectivity: See How Coolbi Optical Engines are built"



Samtec 12x28Bbps Firefly Transceiver YouTube:
"Interview with Kevin Burt of Samtec OFH 2015 HD"

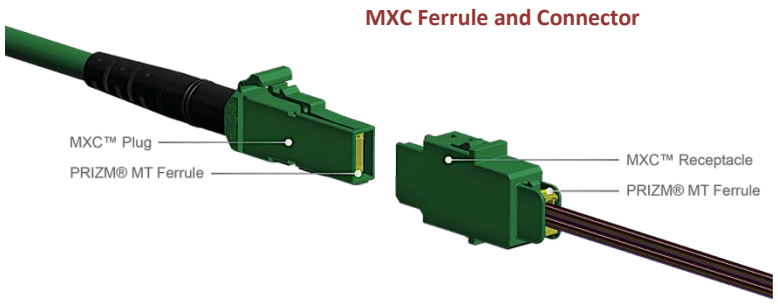
ROADMAP OF QUANTIFIED KEY ATTRIBUTE NEEDS

Table 1.2 Technology Roadmap: MXC
Single Mode Fiber Optic Connector

Notes: SM will be the only solution for 100-1000GB. There are no known roadblocks. MXC/MPO/MPX will migrate to future Multi- Fiber SM Designs w

40-100G LAN Server Storage Switch Router Data Center Other	Package	Type	Multi-Fiber Cable Connector - Rect. Plug – Rx/Tx RJ45-type Latching Interface Plastic Housing				None	Ind. Standard
	Configuration	Type	Cable Assy, Plug, Receptacle, QSFP-MPO Fan-Out Cable					
	Multi-Fiber	Fiber Type	-	MM (SM)	SM	SM		Disaggregated Rack Servers 1.6-6.4Tb/Cable
	Insertion Loss	dB	1.2 – 1.5					
	Max Fibers	Number	-	12	12-64	12-64		
	Cables	Mm OD	-	2.00 – 5.50				
	Compatibility	Types	-	MPO/MTP QSFP LC				
	Housing	Type	Engineered Polymer					Mat'ls Evolution
	Ferrule	Type	MT Expanded Beam					Japan - US
	Attenuation	dB	-	1.2-1.5				
	OPCB App	Y/N	Y – Module, Transceiver, IO, Fly-Over				N Embedded	OPCB Devel.
	Speed/channel	Gbps	-	40	100	100+/Fiber	None	Fiber-Dependent
	Alt. Technology	Type	MPO, QSFP, LC			New MXC	-	Beyond Cu
	Tech. Issues	Type	None				None	SM Field Assy.
	Supply Chain	Type	NA, Japan, TW			NA	Global	Need NA Infra.
	Encroachment	Type	10G Cu	25G Cu	40G Cu	-	-	SiPh Integration
	Cost	$/Fiber Interconnect	1.00	0.75 (10K)	0.50 (100K)	0.25 Millions	Fiber Installed costs > 40Gb inherently lower	Volume Dependent & Speculative
	Mfg. Process	Type	Insert Molding				None	None
	Showstoppers	Type	None				None	

US Conec



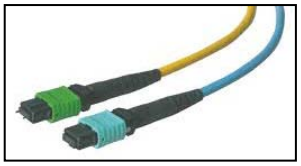


Table 1.3 Technology Roadmap:
MPO Single Mode Fiber Optic Connector

40-100G LAN Server Storage Switch Router Data Center Other	Package	Type	Round Cable Connector - Rect. Plug – Rx/Tx Interface				Cost Target	Ind. Standard
	Standards	IEC-TIA-Ind.	IEC1754-7, TIA/EIA604-5				NA Mfg. Infra-Structure	
	Multi-Fiber	Fiber Type	SM (MM)					10Gx16 72 Count Avail. Future SM Fibers to ≥ 1Tbps
	Fiber	um	50/125, 9/125					
	Max Fibers	Number	4-24	4-24 (72)	4-24 (72)	4-24 (72)	MPO Handles SM w/Push-Lock Design	
	Wavelength	nm	850/1310	1310				
	Housing	Type	Engineered Polymer					
	Ferrule	Type	Ceramic, Plastic					Japan
	Attenuation	dB	0.3-1.0	0.3-1.0	0.15-1.0	0.1-1.0		-
	OPCB App	Y/N	Y – Surface Transceiver Interconnect				N Embedded	OPCB Devel.
	Speed	Gbps	10	40	100	100+/Fiber	None	Fiber-Dependent
	Alt. Technology	Type	Cu QSFP+			New MPX	Improved Cu	Nothing > 40Gb
	Tech. Issues	Type	None				None	-
	Supply Chain	Type	NA, Japan, China			NA	Global	Need NA Infra.
	Encroachment	Type	10G Cu	25G Cu	40G Cu/Fiber	>1000T SM Fiber	-	SiPh Integration
	Cost	$/Fiber	1.00 @ 1K	0.75 @ 10K	0.50 @ 100K	0.25 @ Millions	Market	Volume
	Mfg. Process	Type	Bench/Field Assembly Insert Molding			In Line Automation	-	Injection Molding
	Showstoppers	Type	None				Highly Integrated SiPh will Change Packaging	

Notes: SM will be the only solution for 100-1000GB. There are no known roadblocks. MPO/MPX will migrate to future multi- Fiber SM Designs incl. Ribbon, Waveguide

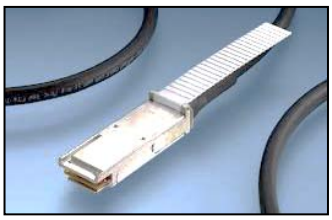


Table 1.4 Technology Roadmap
Active Optic Cable Assembly (AOC)
PSMC Consortium 2000-2025

40-100G LAN	Package	Type	Round Cable Rect. Active Connector – Rx/Tx Interface				Future Cost Targets	Ind. Standard
	Standards	IEC-TIA-Ind.	SFF8470, InfiniBand/FibreChannel, QSFP+					
	Multi-Fiber	Fiber Type	MM (Future SM)					Turnkey Design – Internal Rx/Tx 4x10Gbps @ 100m
	Fiber	um	50/125					
Server	Max Fibers	Number	4	4	8	16	Transceiver Design w/ SiPh	
	Wavelength	nm	850	850	1310			
	Housing	Type	Metal					Plastic?
Storage	Ferrule	Type	Ceramic					Japan
	Attenuation	dB	0.3-1.0	0.3-1.0	0.15-1.0	0.1-1.0		-
	Length	m	100		200	1000		
Switch	OPCB App	Y/N	N – I-O Interconnect				N Embedded	OPCB Devel.
	Speed	Gbps/Pkg.	40	100	400	>1000	None	Fiber-Dependent
	Alt. Technology	Type	Cu QSFP+			PCB Module	None	Nothing > 40Gb
Router	Tech. Issues	Type	None				None	-
	Supply Chain	Type	NA, Japan, China			NA	Global	Need NA Infra.
	Encroachment	Type	10G Cu	25G Cu	40G Cu	-	-	SiPh Integration
Data Center	Cost	$/Fiber	5.0 @ 100s	5.0 @ 100s	4.0 @ 1000s	2.0 @ 100Ks	Market	Volume
Other	Mfg. Process	Type	Bench Assembly InP Transceiver			In Line Automation	SiPh integration	Future Insert Molding
	Showstoppers	Type	None				Highly Integrated SiPh will Change Packaging	

Notes
above: AOCs employ miniature transceiver module technology which will migrate to the next level of heterogeneous transceivers. SM will be the preferred design for TB systems. There are no known roadblocks here, but cost/volume will be an issue. Board-level transceivers are an alternative – with passive cable assemblies.

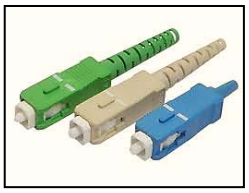
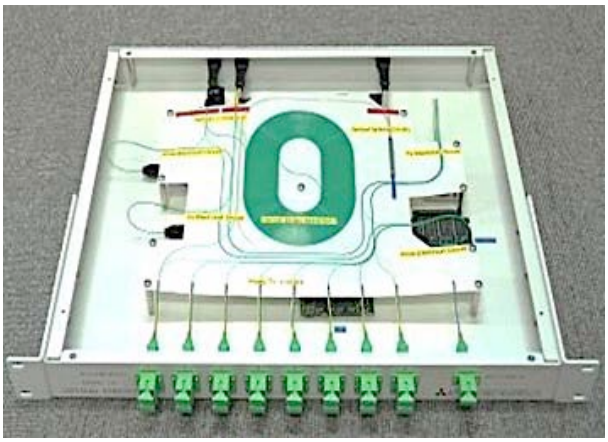


Table 1.5 Technology Roadmap
Generic MM to SM Fiber Optic Connectors 2014-2025

Notes: Mature technology. Bridge to future SM designs. May provide best alternative to board-mounted/embedded OPCB

Mitsubishi Cable Concept Photos: L: Router or Switch Fiber Optic Cable Connections; R: Laptop PC Fiber Optic Bus



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10-40G LAN Server Storage Switch Router Data Center CATV Cable Assemblies Backplanes	Package	Types	Rectangular - Round Cable Connector – Plug-Receptacle				Cost Target	Ind. Standard
	Standards	IEC-TIA-Ind.	LC, CS, Various				NA Mfg. Infra-Structure	
	Multi-Fiber	Fiber Type	MM (SM)					10Gx2 Future SM Fibers to ≥ 1Tbps in New Designs
	Fiber	um	50/125, 9/125					
	Max Fibers	Number	2	2	4	4		
	Wavelength	nm	850	1310				
	Housing	Type	Engineered Polymer					
	Ferrule	Type	Ceramic, Metal					Japan, NA
	Attenuation	dB	0.3-1.0	0.3-1.0	0.15-1.0	0.1-1.0		-
	OPCB App	Y/N	Y – Surface Transceiver Interconnect				N Embedded	OPCB Devel.
	Speed	Gbps/Pkg.	10	40	100	400	None	Fiber-Dependent
	Alt. Technology	Type	Thunderbolt, USB			New Conn.	Improved Cu	Nothing > 40Gb
	Tech. Issues	Type	None				None	-
	Supply Chain	Type	NA, Japan, China			NA	Global	Need NA Infra.
	Encroachment	Type	10G Cu	25G Cu	40G Cu	-	-	SiPh Integration
	Cost	$/Fiber	1.0	0.8	0.5	0.1	Market	Volume
	Mfg. Process	Type	Bench/Field Assembly Insert Molding			In Line Automation of	China Cost Assembly	Injection Molding
	Showstoppers	Type	None				Highly Integrated SiPh will Change Packaging	

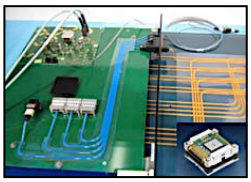


Table 1.6 Technology Roadmap
Generic High Perf. (≥ 10G) Backplane Connectors 2000-2025

Notes: Backplanes are getting both bigger (High Bandwidth) and smaller (Low Power Micro). Bandwidth, Cost Driving BP applications toward FO

Central Office Base Stations Switches Routers Servers Data Centers Backplane Mid-Plane	Package	Type	2pc Box TH	2Pc Box TH ~Fiber	2Pc Box TH ~ Fiber	2Pc SMT More Fiber	2 Pc SMT Most Fiber	Simplification, FO, Cable-based
	Standards	Ind.	IEC, IEEE, VITA, PICMG, other					
	Pins	≤ #	120	200	200	200C 12F	200C 24F	Max. Cu Pin-count
	Pitch	≤ mm	2	2-10	2-10	2-10	2-10	
	Housings	Type	Eng. Plastic	EP	EP	EP	EP	
	Voltage Rating	≤V	100	100	100	0-100	0-100	
	Current	≤A	1.5	2.0	2.0	2.0		
	Temp.	≤C	70	85	85	85	85	
	Frequency	≤/Lane	1	10	10	25-100	100-1T	25-40Gb Cu Max.
	# Lanes	/Gb	2/1	2/4 2/25 1/40.QSF =40gbps 2015 4 channels or Duplex Fiber				
	Issues	Type		Speed vs Trace Design, Signal Length TH vs SMT Shift to Fiber Optics & SM?				
	Supply Chain	Where	EU-NA	NA--CN	NA-CN	NA-CN	NA-CN	NA HVM Infrastructure
	Encroachment	Type	Hi Performance Cu (MM Fiber)			SM Fiber	SiPh	Future SiPh Systems
	Other	Type	Backplanes transitioning to Cabled, Low Voltage and Fiber, 2020s replaced in future SiPh systems					

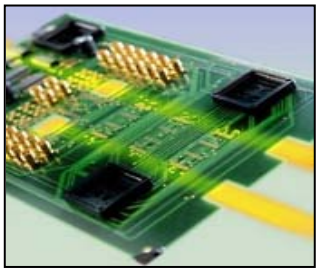
Layers Range 6 to 72
Board Thickness 2.5 mm to 12.5 mm
Board Size Range 100 mm to 800 mm per side
Length to Width 1.5:1 to 3:1
Device Pitch 0.5 mm up to 2.5 mm
Typical Materials FR4, HF FR4
Material Thickness 0.075 mm to 0.450
Buried Capacitance YES, needed for power Integrity Source:
Voltages Multiples up to 8
Source: IPC 2015 Roadmap Draft

Signal Integrity Controlled impedances, long signal lengths
Typical Through-holes 0.200 mm to 2.540 mm connectors, pins, back drilling
Typical Components Connectors, devices like opto-coupler Interconnect
Cables - copper or optical
Design Rules: L/S: Via/Pad: 0.075 mm to 0.150 mm / 0.100 mm to 0.250 mm 0.100 mm to 0.250mm / 0.200 mm to 0.450 mm Via Stack 1
Buried Components EP resistors and capacitors
Power Dissipation Can be very high, heat sinks-cooling schemes, now thermally conductive laminate

Table 1.7 Technology Roadmap Discrete Optical Interposers
PSMC Consortium 2014-2025

Photos: L Molex HBMT FO Backplane Connections
R\R: SPIE FO Connections to Storage rack

Molex Fiber Optic Connectors



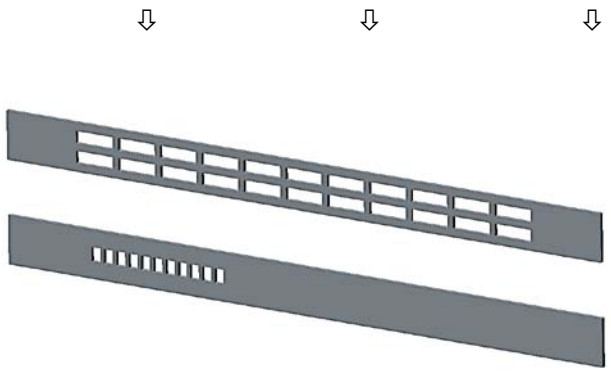
Optical Interposers are sockets or fibered modules with EO conversion from a Cu CPU/ASIC or SIP-SOC mounted to transceiver-based socket. Optical output is currently discrete MM fiber cables. Future: OPCB Optical Connections: Embedded Waveguides in Si Packaging, Expanded Beam technology may be integrated into future SIP designs	Package	Type	MBO PCB Module	MBO PCB Module	Future Socket/SIP	Future SiPh Pkg.	MBO is an elegant Interim Solution to Ph Conversion from a Cu Si Chip/Chip Pkg. It will evolve into a Socket with above board Optical Interconnect and/or a package-integrated Photonic Interposer . Issue: No Viable FO Direct Attach to Future OPCB. Probable: Integration into SIP and eventually SOC Currently Capable: 100-400Gbps Future SiPh: >1Tbps.
	Standards	Spec	QSFP+	QSFP+	New	New	
	IO Pins/ports	#	≤12	≤12	≤12	WDM	
	Pitch	mm	>2	>2	>2	>2	
	Housings	Type	Metal	Metal	Plastic	Plastic	
	Voltage Rating	V	5	5	5	5	
	Current	A	<2	<2	<2	<2	
	Temp.	C	85	85	85	70	
	Frequency	Gb/Pkg.	40	100	400	1000	
	Issues	Type	MM	MM	SM	SM	
	Supply Chain	Region	EU,NA,AP	same	NA	NA	
	Encroachment	Type	Cu	Cu (MM Fiber)	Cu (SM Fiber)	SM Fiber/SiPh	

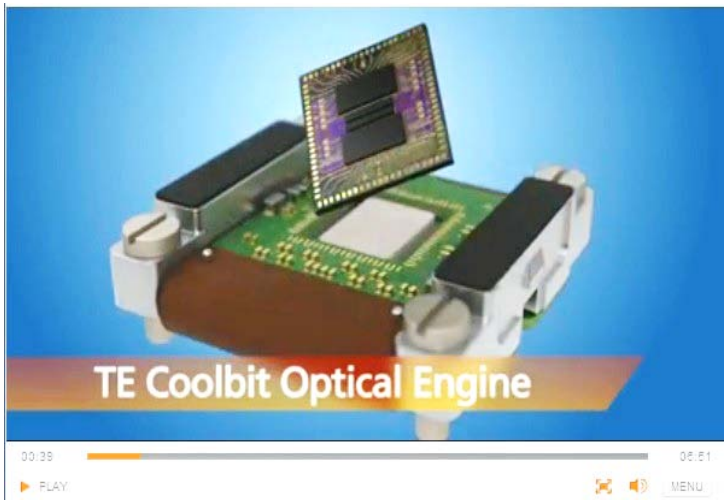
Semiconductor fabrication of VCSEL and Photodiode ICs…To Wafer Assembly of ICs with passive self-alignment and Test. As speeds increase to 25GHz, the number of signal compensating electronics needed is skyrocketing along with costs. As a result, an emerging product segment has been created that allows system designers to embed optical transceiver technologies inside computer and communication systems. Embedding high-speed optical transceiver technologies, known as mid board optics (MBO), onto traditional server line cards or switch fabrics allows system architects to achieve:

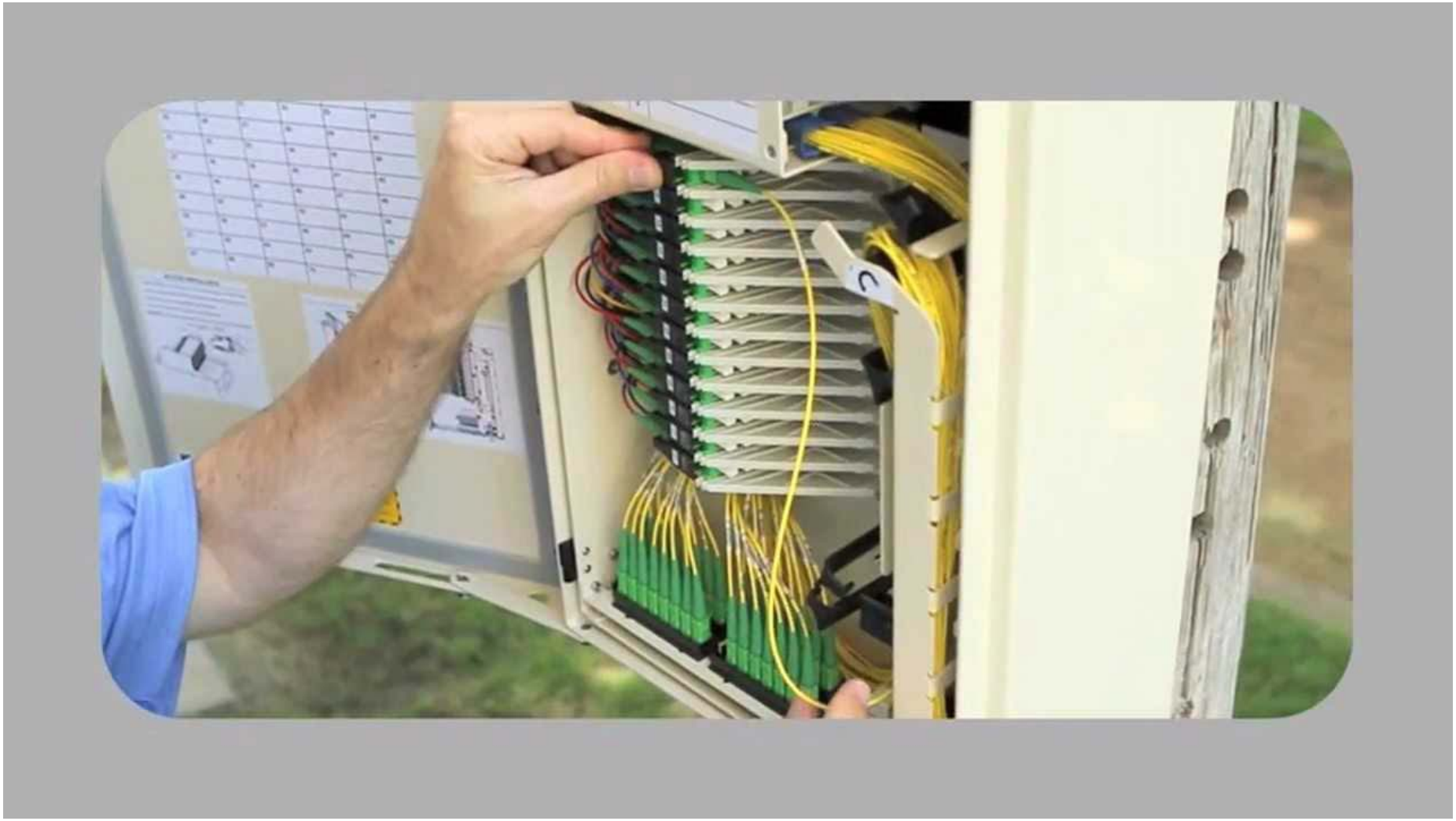
- Higher input/output densities
- Systems that are not bound by copper interconnect lengths
- More power-efficient systems

MBO inside systems mitigate the added electrical losses encountered at the 25 Gbps signaling rate. Figure below shows a comparison of faceplate density when optics move off the faceplate and onto the system's printed circuit board. The top image shows maximum pluggable I/O density, based upon 400 Gbps CDFP active optical cable assemblies.

The bottom shows the benefit if I/O is based upon optical connectivity. The optical solution results in substantially higher electrical I/O density while eliminating the cooling problem at the faceplate. The top design in Figure 2 has 22 CDFP MSA x 400 Gbps. The bottom faceplate has only 10.







Connectivity Mini Fiber Distribution Hub (youtube.com TE Mini FDH)

Table 1.8 Organic Printed Circuit Board Photonics Roadmap 2014-25

Workstation **Server** **Scientific Computers** **Super Computers** **40GbE – 1TbE LAN/WAN** **Storage Farms** **Data Centers** **Routers** **Switches** **Base Stations**	# Suppliers	Number doing HVM	0	0	2	10	OEM Buy-In	If Bandwidth Flat lines @100Gbps
	Laminates	Type: FR4 - Other	FR4	FR4	OFR4X	OFRX, OBT	SiPh Develop.	Superseded by New SiPh SiP/PoP Substrate technology
	Embedded Glass Fiber Layer	Type	Fly-Over FO Cables	Fly-Over FO Cables	Fly-Over + FO Sheet	Fly-Over + FO Sheet	Inner Layer Fiber Interconnect	Shift to SiPh Substrate above reduces need for outboard OPCB
	1st Year Mfg.	Type	2000 Devel.	Initial Prod.	Mid Vol. Mfg.	HVM or New SiPh Substrate	OEM Timing, Commitments, IP	Key OEM Leaders Develop 'Competing' Proprietary System-Level Technology
	OPCB Connectorization	Type	Cable, BP, IO, AOC	Cable, BP, IO, AOC,	Initial OPCB Conn. MXC?	OPCB MXC? MPO?	Embedded Fiber Connectorization	SiPh Micro-Interconnect Substrate & Interconnect System?
	Embedded WG	Material	Silicone	Silicone	Silicone	Si, SiPh Deposition	Embedded WG Connectorization	Bandwidth/Speed/Cost?
	OPCB – Year HVM	Type	Develop.	Prototype	Initial Mfg. – Emb. OPCB	HVM Emb. WG, SiP/SiPh	Mfg. Cost?	Tb Speed will Require PSMC Micro-Packaging System Goals
	Embedded WG Type	MM-SM	MM	MM	MM Silicone	SM WG?	SMWG?	Can/If < 20mm WGs need be SM
	WG	V – RA – IO Only	None	None	IO	RA, IO	RA Embedded	Cost, HVM
	Embedded Fiber	Gbps MM - SM	25 - na	40 - na	40-1000	40-10^6	None	None
	Embedded WG	Gbps/mm	na	na	25 @	100 @	Unknown	More associated w/Module/SiP Packaging
	Embedded Fiber dB	dB/km	na	na	3-0.4	3-0.2	3-0.2	None
	Embedded WG	GHz	na	na	25	100	100	Mat'ls Devel.
	Embedded WG dB	dB	na	na	0.1	0.05	HVM	Mat'ls Devel.
	OPCB Connector	dB	na	na	1.0	0.5	None in SM	None
	Min Lines/Spaces	Cu-WG nm	60-na	50-na	30-250	20-100	Embedded WG?	Inner Layer WG beyond SiP?
	Comment: PCB Internal WG Layers is in Late Stage Develop./Early Stage Mfg. Issues: There is currently no Industry Develop. Work on OPCB Connectorization to Embedded Optical Layers or Fibers. Fly-Over Optical Fiber Used Today – MM and SM and is an efficient, high bandwidth alternative.							
	Comment: Future PSMC System will Supersede Interim developments ~ Highly Integrated, Wafer or Panel-Scale CPU/ASIC Process w/ SiPh Engine; Etched Glass or Waveguide Structure, Optically Connected via Socket or Off-Chip Micro Connector to a System Platform = Organic PCB w/Discrete Micro-Ribbon Cables, System Board FO Connectors and AOCs for < 1Km Intra-system Interconnects							
	Comment: i.e. The PCB becomes the Physical Platform for a Highly Integrated Optical SiP which May include the CPU/ASIC to Provide End-to-End Optical Communications. Focus may be on micro-electronic packaging – not motherboards or daughtercards which may eventually be obsoleted by SoC/SiP							
	Comment: HVM Disaggregated Data Centers for the Fortune 500, Major EDU, GOV and Military. Servers, Scientific/Mainframes, Large Workstations, Switches, Routers. DWDMs							
	Comment: Most SiPh apps will be rack & IO-based. Question is when Cu in packaging will give way to end-to-end Photonics. i.e. 2018-25							
	Other Key Technical Specifications: on PCB technology are well documented in IPC 2015 Roadmap							
	There are currently only 2 IDed domestic PCB mfrs. With OPCB developments. The domestic HVM PCB industry is moribund: Taiwan, Japan, China OEMs + Outsourcing							
	The connector industry is 'Wait and See' on embedded WG to surface layer FO connector. Prefer fly-over options which can be upgraded to SM							
	FO backplane connectors to Backplane Boards are well-developed, but most efforts have been to High Speed (10-40Gbps) Cu. BPs may be future dodo bird: e.g. Cabled Backplanes or PCIe Micro-Server Motherboard							

Organic PCB Roadmap Comments:

Organic Interconnection PCBs are 100% copper-based. As photonic requirements become important, the PCB industry will grapple with a disruptive technology that most PCB suppliers are unfamiliar with and are unprepared to deal with from both technological and investment capabilities. The first step toward photonic capability, already in existence, will be to use discrete 'fly-over' optical cables as shown in the illustration on the previous page. The next step, proven out by IBM, DOW Corning and a handful of PCN makers, will be to employ polymer waveguides in surface layers, and then (as needed) there will be embedded waveguides on inner layers with optical via structures connecting to surface-layer optical receptacles.

Currently, most organic PCBs consist of different sized substrates and include substrates for Modules, Portable Boards, Product Boards (i.e. daughtercards and motherboards) and thick multilayer Backplanes. High volume IoT products will be driven by a range of PCBs from simple double-sided boards to high density, thin 'HDI' and alternatively low cost structures. These PCB's may be woven into clothing and embedded into non-traditional products. The cost expectations from the Product Sector Emulators may be difficult to achieve in North America or Europe, as will be the transition to photonics. This will be aided by supplier input such as from DOW's silicone materials.

In today's market, the so called standard FR-4 is gradually disappearing. The replacement is still an epoxy, resin based material, however, the resin fillers and inclusions of other resin makes for a variety of choices. Higher speed/low loss systems are substituting PPO and other resins for FR4 to increase the signal speed and replacing glass with low loss reinforcements and novel weaves.

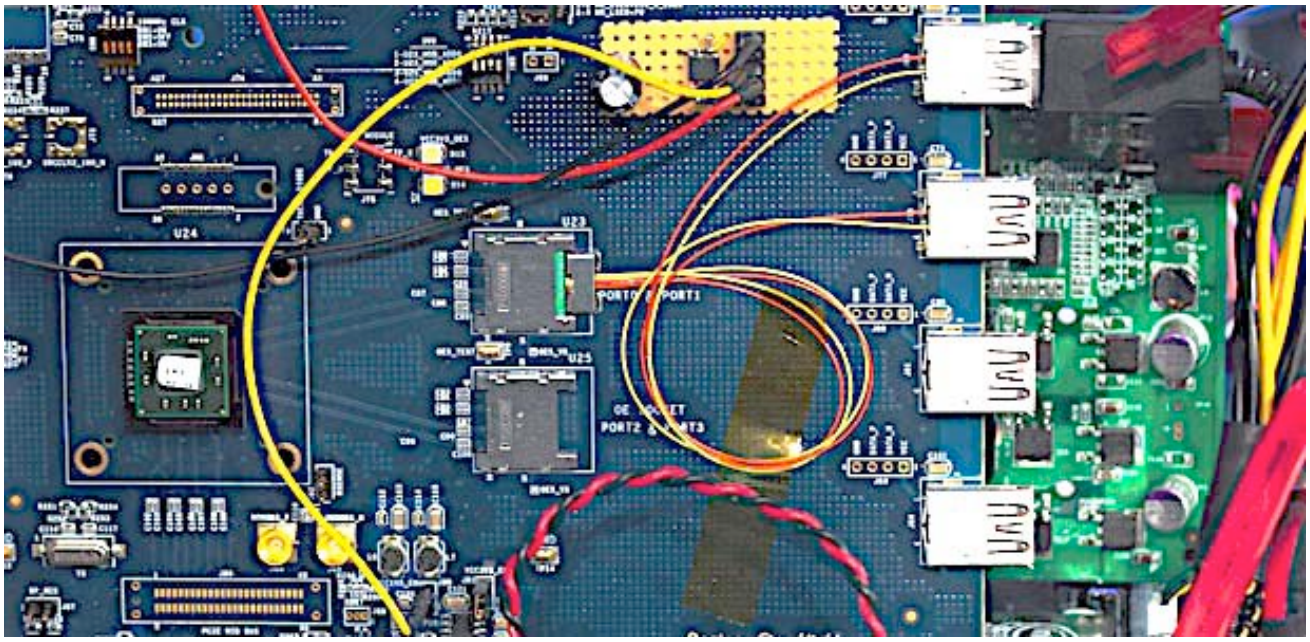
The drive toward lead-free soldering along with more environmentally friendly materials and processes have changed the surface finish and material characteristics for the printed board delivered to the assembler. Some proponents of the issues suggest that recycling, or take-back requirements, are a more desirable solution for the environment as opposed to lead-free and newly-restricted bromine free products. These conditions are being explored and discussions are underway on how products should be labeled in order to assist the recycling efforts.

Environmental organizations are pushing to eliminate certain bromines as a flame retardant in laminates while the move to lead-free solders means higher soldering temperatures that the printed board must withstand. Generally, laminators all over the world have developed different replacements in order to meet the high temperature requirements needed in the assembly processes. A new requirement for laminate is the time to decomposition (Td), and is being used to define the process temperature window. The higher the Td, the greater the number of exposures the material can survive in the assembly process. With all the changes in the substrate chemistry, the risk on long term reliability or substrate degradation continues to be of concern. More custom versus generic material development is creating high volume materials optimized to the product form factor and environmental conditions to minimize the cost.

Passive and active components are buried inside the printed circuit board as needed for both wiring density increases and for electrical performance reasons. There are several activities in the industry that are developing processes that address the simplification of these processes since sequential process steps, usually incur additional costs. The CAD systems and the board fabrication infrastructure are not as ready as they need to be in order to have full implementation.

As reduced product life cycles continue, there is discussion about application specific reliability requirements that could affect board reliability testing. There is a certain amount of confusion as to who is responsible for the testing. With all the OEM outsourcing of board and assembly manufacturing, the decisions for Burn-in, HASS (Highly Accelerated Stress Screening) and HAST (Highly Accelerated Stress Testing), is an ongoing discussion between customers and suppliers.

The Printed Board industry is no longer dominated by captive fabrication facilities. It is an industry dominated by several large independent global board fabricators, with today's model of the EMS giants acquiring printed board fabrication facilities. China manufactures the highest percentage of PCB's for most board types. But, their cost advantage is being challenged as labor and infrastructure costs increase significantly. This is driving the industry to move high volume manufacturing to lower cost regions in southeast Asia, but so far not to 'Insource' back to North America or Europe.



Intel believes that Light Peak, its high-speed optical interconnect technology, will be integrated within all PCs and consumer electronic devices in the next couple of years, thus catapulting optical technology from the relatively niche telecom market to the mainstream. (Source: teledynedaisia.com and Lightwave Magazine.)

Note that in this case – as in all others at this time, transceivers are with above board 'Fly-Over' cabling. Given FO's use as a Fiber/Cable Connector, Factory-Terminated Cable Assemblies, Active or Passive, is a good solution for mixed FO and Electronic Circuitry – and can provide SM solutions now.

CRITICAL INTERCONNECT ISSUES IN THIS PROGRAM

Generally, FO Connectors and Cables will be able to meet SiPh technology challenges because optical fiber technology is well advanced with unlimited bandwidth capabilities and has mature, well-established interconnect technologies built upon 35 years of experience in the telecommunications industry and more recently datacom.

Copper-based circuitry has advanced well beyond earlier capabilities too, and will continue to advance toward 100 GB throughput for short ~1m distances. These improvements lead some people to believe FO is not a major priority inside the box. They have been burned before by premature FO hype, and believe Cu-based design tools have captured the electronic packaging market well into the future. There are those working diligently on optical fiber solutions, but the number of companies doing this in the connector and PCB industries $\leq$ 10. There are a lot more making cable assemblies. At the core of optical fiber is one major US company, Corning Glass.

- **Industry Cooperation**: Getting cooperation from industry personnel is difficult because of perceived IP issues involving their customers. The connector and PCB industries are very much revenue-based in their work – and have fewer R&D personnel than in the typical semiconductor business. The number is far less than a decade ago due to globalization. We basically have an industry with scattered proprietary projects, sole source positions and high profitability on these items, which may or may not be a prelude to HVM.
- **Cost Targets**: Proposed cost targets in a maturing industry are viewed as unrealistic for FO connectors unless standards are developed for products yet to be mfd. in HV - standards that would remain stable to allow for automation, which so far has not been used extensively in FO connector mfg. There is also an issue with tooling investment - until there is a proven market backed by specific major OEMs. Use of existing standard products in FO connectors and cable assemblies may be helpful in this regard, but manufacturers are suspicious of commoditization trends with standard products that can be 'knocked off' by Asian competitors.
- **Entrenched Global Supply Chain**: FO and PCB mfg. have evolved to where most of the components and materials are part of a global supply chain. It would be difficult to sever those arrangements, yet the NIST funding envisions a domestic mfg. infrastructure. Same goes for tool and die work, assembly equipment, mold tooling, FO connector ferrules; and HVM of *domestic* organic PCBs and IC packaging substrates. In the PCB area 90% of HVM is in Asia – even among the 5 or so major US PCB firms.
- **Level 1-2 Interconnects**: Connectors at and near the chip are rare and IC sockets are being replaced by direct solder-attach of CPUs and memory. There are interim FO Rx/Tx module solutions on the market now that convert chip electrical signals to optical fiber, (TE Cool Bit, Samtec, Molex and FCI); but what is envisioned by PSMC is a SiPh SiP or SoC that will require internal micron-level chip or substrate waveguides to external mm optical fiber interconnect. OEMs may not cooperate except with suppliers who have signed IP and secrecy agreements; and accept OEM-proprietary design ownership with license to make parts for them. So this is a difficult area to get input, where we believe there are technology roadblocks to achieve these optical fiber/waveguide interconnects.
- **OPCB Interconnects**: Optical PCB technology is in the development stage at TTM, IBM/DOW and possibly elsewhere. However, the domestic market has been decimated by offshore competition and has limited capability to take on new technology. In addition, an OPCB connector, i.e. board mounted to embedded fiber or waveguide layer, is not in development by connector manufacturers. Angled micro-mirrors or other optical micro-via solutions need to be developed for HVM of an OPCB connector, and there needs to be cross-industry cooperation for

both the OPCB and OPCB connector to happen. Otherwise, optical fiber routing at the board level will remain discrete above board cabling, which is not necessarily a bad thing.

- **SM connectors**: Are well developed, but their use has been in mostly factory pre-terminated designs and in small to mid-volume production. While this is not a major technologic issue, it does bear on cost and reliable, efficient field termination of SM connectors.
- **Applications Closest to the Chip:** Difficulty increases in proximity to chips: i) the connector industry is not well experienced at this level, which has typically been proprietary to the semiconductor industry, ii) feature sizes are below those capable in the merchant connector industry, iii) use of discrete fiber optics compounds these issues. There is fine work being done at IBM and Corning's US Conec, and several connector makers have developed postage-stamp sized transceivers. However, this is a volatile area, subject to rapid encroachment by SiPh solutions that will subsume discrete connector applications. For the time being, InP transceivers at the board and active cable assembly level, and developments in optical interposers are on-going.

PARADIGM SHIFTS:

Paradigm-shifting technologies will occur above the connector industry in the OEM ranks – and will result in new FO connectors and cable assembly applications as required by these new system-level developments. One connector paradigm would be the introduction of lights-out automation for a future low cost FO connector – to be the "USB" of the SiPh system technology.

- **Commercial HVM of Silicon Photonic ASICs and CPUs:** As this happens there will be an accelerated paradigm shift toward optical interconnect and packaging inside the box. It will be most rapidly adopted by Intel or possibly other chip-makers.
- **Commercial HVM SiPh Chip Packaging:** Spinning out of current System-in-Package/3D packaging technology, this will come before a SiPh System-on-Chip solution but it is unclear who is working on this: Packaging firms or chip OEMs such as Intel. The TE Cool Bit transceiver module solution is there now – as a separate Rx/Tx package capable of >400Gbps through 4 channels.
- **Commercial HVM Optical PCB Technology**: As discussed above – with embedded waveguides and an OPCB connector solution. This is a 'chicken-egg' issue between the connector and PCB industries and their OEM/EMS counterparts.
- **HVM** (100Ks – Ms) **vs. Low Volume** (100s – 1000s) **Manufacturing of SiPh systems**: There may be a tendency for this work to result in lower volume specialty/proprietary manufacturing of Routers, Matrix Switches and other products, rather than the paradigm shifting release of SiPh systems for HVM. OEM buy-in will be critical for a HV/SiPh/M paradigm to occur.
- **Domestic US HVM Infrastructure**: There is a good chance for this technology to ramp domestically for several reasons: i) It is new technology, ii) The US has the semiconductor infrastructure, iii) Major system OEMs are here, iv) The biggest market is here, v) Si Valley is known for innovation, vi) World-class University research in this area is substantial.
- **Supply Chain Infrastructure**: This area is geographically diverse and may not be as critical to a dominant US SiPh industry as will be the semiconductor and packaging technologies. Connectors and OPCBs will be a mix between domestic and international capabilities – particularly from the EU and JP. A shift away from China is already underway due to many factors.

STATE OF HVM IN US ELECTRONICS MANUFACTURING

HVM in the US is mostly limited to semiconductor manufacturing – but there has been a slow leakage of manufacturing to offshore facilities, including Silicon foundry operations in Taiwan and Korea. HVM of automotive connectors to a great extent remains here except to the extent that US auto companies are global in their mfg. footprints. Mid-to-lower volume mfg. of connectors and printed circuit boards remains here, including specialty products and Mil/Aero. Most US manufacturing industries have experienced offshoring to one extent or another, but the term "Offshoring" is inaccurate in the sense that system assembly is what drives component manufacturing, and it is system assembly that has been outsourced and moved to low cost labor areas. That tide appears to be turning, with some predicting China's run as the HVM source for the industry is beginning to fade – and will more so as advanced robotic assembly takes hold in North America and Europe. But this will take time and concerted efforts by industry and government to reverse years of chasing low cost labor as an alternative to investments in high volume automated production. The HVM issue is constrained by short product life cycles and risks associated with large capital investments. Thus, issues here abound – including, the outsourcing of manufacturing to EMS firms who work on thin margins and have long established assembly plants in Asia, and the fact that most large component makers have been global in their manufacturing footprints – of necessity to support EMS firms and gain market share internationally. These companies now have an embedded global operating culture with organizations networked around their global supply chains and customers. Below are graphs of US shipments in various important US manufacturing industries over the past 20 years and projected forward to 2025. These industries use interconnect products:

One can see that with the possible exception of automotive, (which has a somewhat speculative* domestic renaissance in process with hybrid and electric vehicles), these markets have shown limited domestic shipments growth over the period from 1995 to present – and projecting forward. This record is both a reason for new technology initiatives, and a concern about growth prospects in home markets.

Note in particular 20-year shipment trends in all categories to be touched by a SiPh initiative:

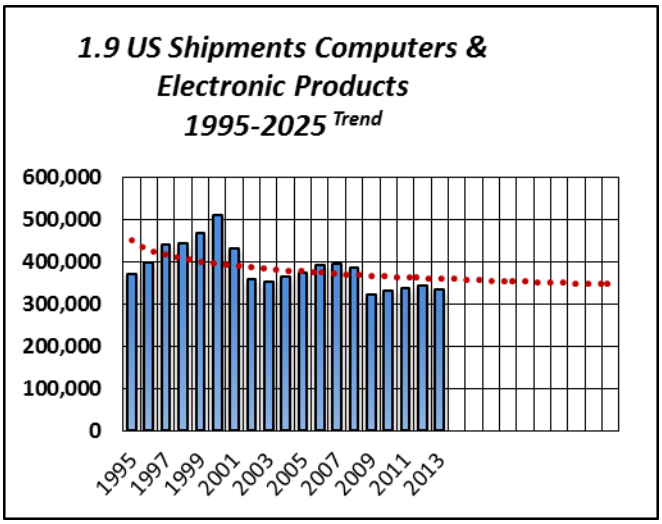
★Electronic Components, ★Semiconductors, ★Computers & Electronic Equipment, ★Communications Equipment and ★Electronic Storage Equipment.

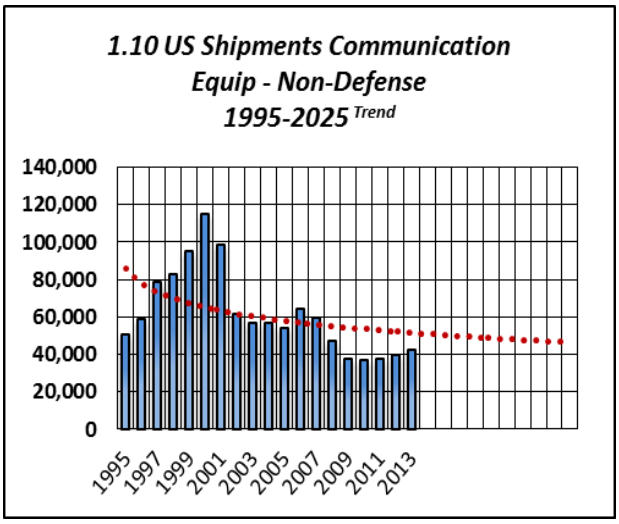
Note: The general picture for US manufacturers is much better to the extent that they have globalized their businesses and now enjoy ~60% of their revenues internationally. In electronics the percent of business in the US has declined from 60 to 40% or less for most domestic businesses. In connectors the US market is now <30% and in PCBs less than 20% of global production.

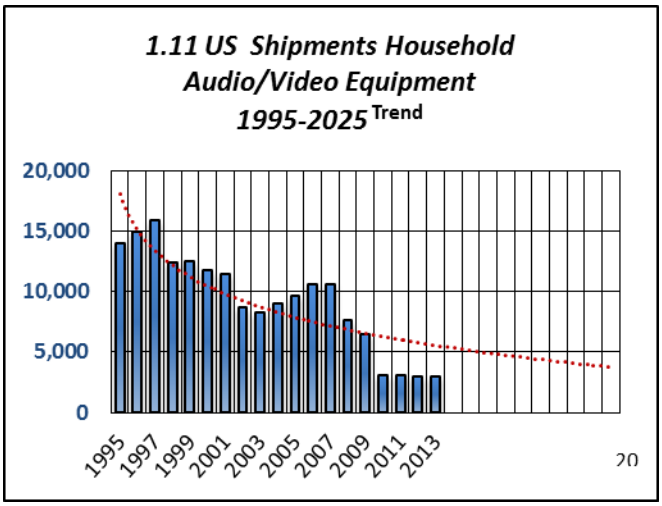
*Subject to Globalization and a future flood of low cost imports

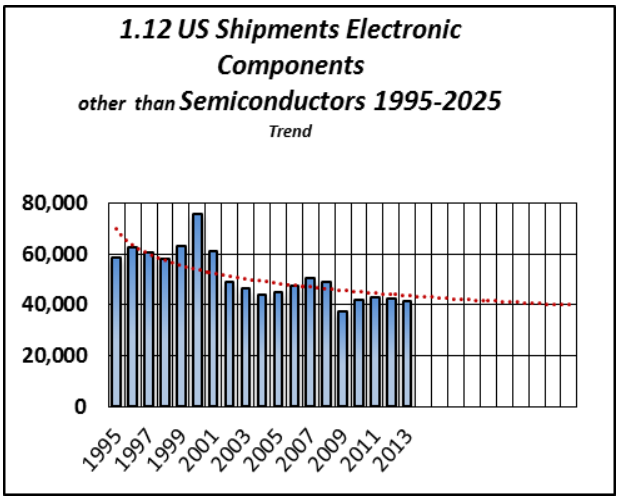
Table 1.9-1.18: US Shipments of Electrical & Electronic Products 1995-2023

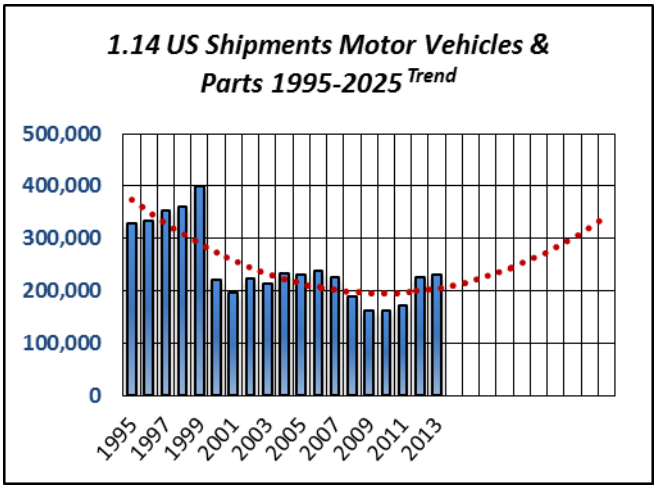
Source: US Census Bureau M3 Data
$ x M

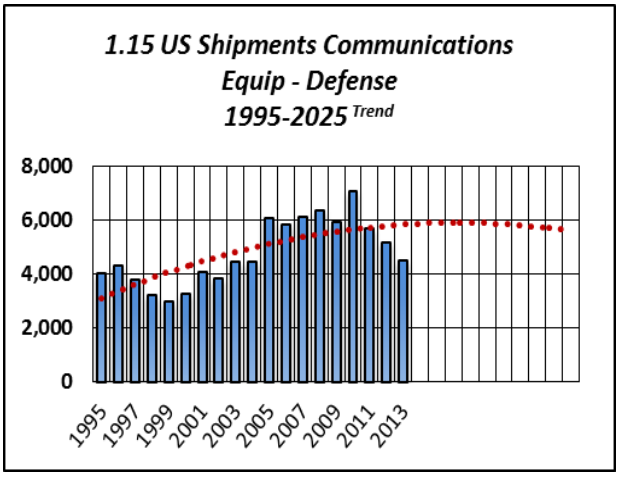


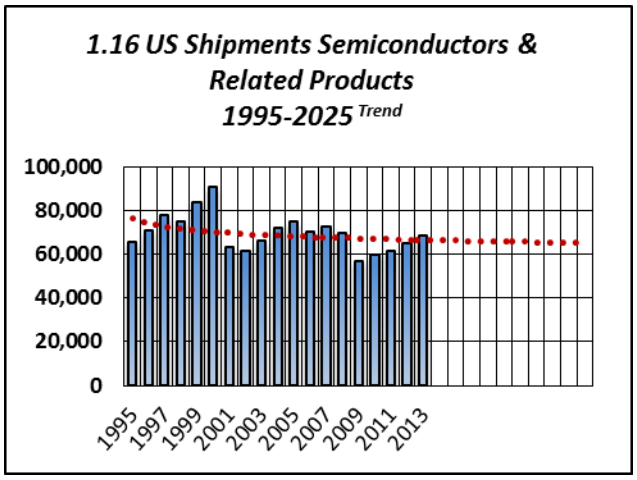


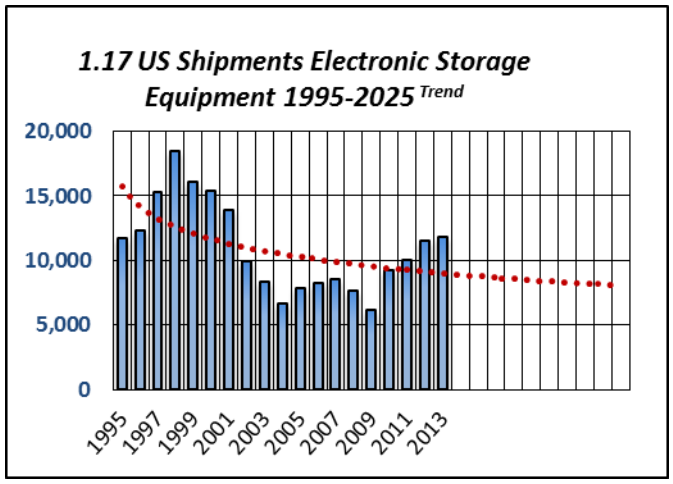


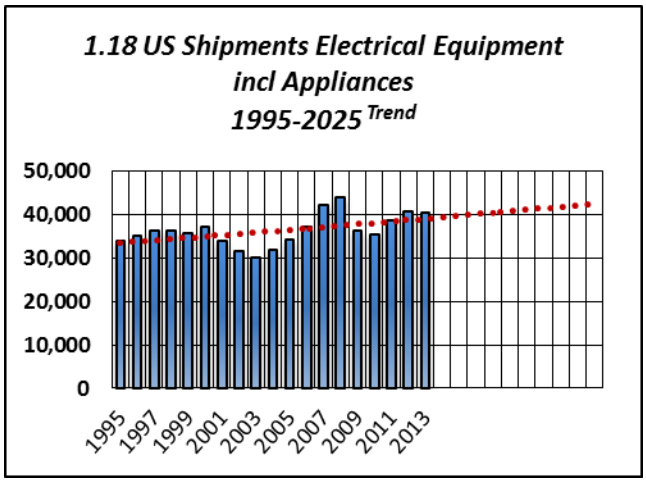












The above tables (taken from Census Bureau data). illustrate the extent to which US shipments of electronic products has changed over the past 2 decades and going forward to 2025. What is not shown in these graphs, but is predominant in all of electronics 'light manufacturing' is that it has been a prime target for offshore manufacturing – and that most electronic component industries have had to follow OEM customers and their EMS/ODM manufacturing partners to China – or else lose the business.

This illustrates the multiple challenges facing this industry and the difficulty in being able to mount major new technologic programs when most if not all HVM is already in Asia. Fiber optics manufacturing may be the exception for both US and European suppliers. But it will require EMS manufacturing partners to OEMs to become proficient in assembling photonic systems, which they are not at this time, and like many food chain suppliers, have limited investment capabilities, as their main electronic assembly businesses run on very thin margins.

FIBER OPTICS TECHNOLOGY

This connector technology is 30 years old – from the earliest days of the FO telecom cable plant. By the mid-80s it was thought that fiber optics would eventually overtake Cu circuitry; but of course that has not happened due primarily to unheard of advances in Cu circuitry. It was not so much improvements in Cu conductors – it was the result of general circuit design improvements, including in semiconductors and signal conditioning. Today the threshold for fiber is in the 10-40Gbps/channel range depending on distance and other factors, with reliable light sources beyond 40Gbps being a challenge. Inside the box, Cu remains the choice in over 95% of all applications save central office and some data center applications. Fiber is used at IO ports and between equipment in data communications, in some high speed backplane applications, and in specialized applications in medical, mil/aerospace and other applications. FO is experiencing renewed growth as it enters applications in electronic packaging – beyond the cable plant.

Background:

Fiber Optic (FO) connectors were originally designed as metallic circular connectors. FO interconnects have since evolved into many different designs and applications – including the long-awaited build-out of Fiber to the Home (FTTH). AT&T, Verizon, Google and others are installing fiber optic high-speed Internet and video systems to compete with slower cable systems – many of which also uses FO in their backbones. Both systems currently use Cu (Cat 5 or Coax) beyond the NID i.e. inside the premise. Thus Fiber-to-the Curb is the correct moniker (FTTC).

FO Growth Drivers: Historically Telecom Plant. More recently High Speed Datacom – signals > 10Gbps >100m; ≥10GbE, Data Centers: Switches, Routers, WDMs, and Super Computers.

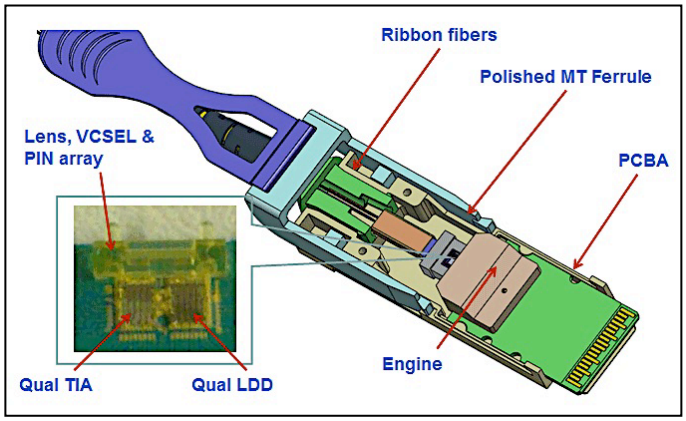
Higher costs than Cu, loss budgets; improvements in Cu performance, and a world of embedded Cu-based electronic equipment applications and design software have limited fiber's use *inside* systems. For the most part electronic systems remain electronic (Cu) from the Si chip interface to the IO panel. But that is changing.

FO Interconnect: Was primarily cable, IO and inter-system interconnects: speed/bandwidth, long cable runs leverage FO's strengths in LAN, campus and outside plant telecom. Future will include Levels 2-5 inside the box, Level 6 IO, Level 7 Inter-System and potentially off chip.

An area with technology overlap between connector manufacturers and transceiver makers exists. In a sense, these modules are no different than OEM products in that connector makers can procure the parts necessary to build these modules.

FO is Moving toward Expanded Use in Hybrid Cu-FO Electronics: Circuit applications from 10-40 and 100Gbps beyond. Tb and Pb speeds within a decade. There are few roadblocks for connectors which are basically contact mechanisms for optical fiber; but, rather an evolutionary expansion of FO technology and applications against firm, long-term experience with Cu. Key to FO expansion inside Electronic Equipment will be developments in SiPh ICs, substrates and SiP; e.g. Intel's announcement of a chip enabling USB-like interconnects with fiber such as Light Peak, and work on direct photonic output from high performance logic chips. Cost is also a major factor; but where Cu runs out of speed, FO is the only viable solution.

QSFP+ Transceiver - 10gtek.com



PCB TECHNOLOGY:

EOPCBs still in Development: There is substantial work at the chip and package level utilizing glass and polymer waveguide structures for distances <1cm. However, the merchant PCB industry has done little development work in FR4-type multilayer boards, (with a few notable exceptions). Existing card-level FO interconnect has typically been above-board round or ribbon FO cables and connections – such as in the few existing FO backplane applications. Thus, this does represent a significant area of development (and commitments to move forward) both at the PCB and SMT/PCB FO connector levels

Table 1.8 FO Deployments:

2011		2018 - 25
▪ Outside Plant. WDMs, FTTC	▪ Base Stations	▪ System Packaging: Servers, Datacom, High End PC
▪ Commercial Buildings	▪ Data Centers. (LAN)	▪ 100-1000GbE
▪ HPCC Intra-system, Equip Room	▪ HPCC, 40GE, Fixed FO IO	▪ Massive Cloud Data Centers
▪ Fiber-to-the Curb: Cable/Internet	▪ Storage Equip: SAN/NAS	▪ Datacom/Video Networks
▪ USB 2.X (Cu)	▪ USB 4.0 Light Path (Intel)	▪ Tb Internet Backbone
▪ Copiers, Instruments	▪ Medical Diagnostic	▪ IoT
▪ Special Applications (E-Z Pass)	▪ Industrial Equipment	▪ Automated Highway Systems
▪ Digital Optical Audio (plastic)	▪ Military/Naval/Aerospace	▪ Currently Unknown
▪ Networked Servers Switches Routers	▪ High End Work Stations	

Internecine Roadblocks for Fiber Deployment in System Packaging: i.e. Cu and FO: *will compete* for new high speed, high bandwidth technology applications up to at least 40Gbps and of course there will still be Cu as power is required in all circuitry:

- There will be increasing Cu performance (Circuit Design, Design Tools, and EOICs) but this may be reaching the practical limits of Cu between 40Gbps <100m, 100G < 1m.
- Need Low Cost Optical ICs (Logic, ASIC) and EOPCBs at the chip & package levels.

- Cu circuits meet most existing 'box' applications, all of which require power and signal. As long as Cu continues to meet circuit needs – even with compromises to enjoy its lower costs, it will continue to be used with and without FO.
- Current FO connectors are more difficult to apply and test for quality. Often require non-standard tools. New pre-polished connector assemblies address this issue; but in a multi-vendor/multi-subsystem environment, both in-house and field terminations will be required. Pre-terminated cables solve this issue.

General Roadmap Dialog (2015 iNEMI Roadmap, Robert Hult et al)

Available Elements of a Photonic System:

- Optical Fiber and Cable: multi-mode, single-mode.
- GaAs, InPh Lasers, WDMs, Planar Light-Wave Circuits (PLCs), Silicon and InPh, Transceivers, Connectors, Cable, and other Components. These are addressing high speed Backplane, IO & Inter-System requirements in Gbps realm.
- Waveguides include traditional multi-mode and single-mode glass fiber, high index delta fibers for small bend radii, polymers that can be lithographically patterned, and plastic optical fibers.
- There are multiple I/O connector standards including LC, SC and MPO/MPX/MXC. There are several proprietary backplane connector styles; however these use standard connectors, and are really rear I/O connectors, not the optical equivalent of Cu backplane connectors.

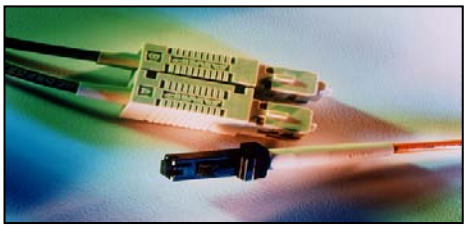
Future Breakthroughs:

- Intel has developed Si Raman lasers, waveguides and hybrid Si Laser sources. This means future systems could be mass-produced with low cost Si optical chips, PWBs with outer or inner layer waveguide/fiber interconnects, lower cost ($/Gb) transceivers and connectors (with HVM at the system level.
- The most likely implementations of a hybrid or all-optical system will be with 3D multichip systems-in-package (SiP), interconnected in controlled packaging environments. 3D Chip stacking technology facilitates integrating optical chip functions. However 20-25 Gb/s Cu backplanes are now available, which will compete with fiber backplanes for the next 2-3 years. Usage of either, or both will be system-dependent.
- Plastic Optical Fiber (POF) has the advantage of low cost LED drivers and very flexible POF cable. It is used in digital audio applications and has the potential to be used in other consumer and industrial applications with relatively short cable runs. It will be a candidate for many premises wiring-related IoT applications.
- Shown below: (L) S/PDIF POF connectors; (R) Calumet Electronics SBIR award to develop embedded SM waveguides for electro-optical PCBs (EOPCB and EOPCBA) from Naval Warfare Center, TTM Technologies OPCB developments (not shown) – portending a future electronic packaging scheme based on optical printed circuit board technology

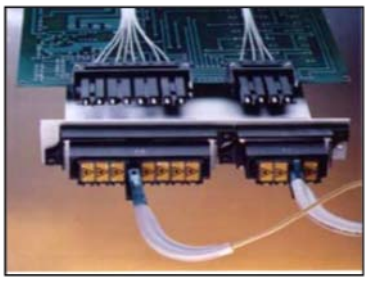
Table 1.19: General Fiber Optic Connector Roadmap (iNEMI.org 2015 Roadmap)

Applications	*Parameter*	*Metric*	*2000*	*2015*	*2018*	*2025*	*Roadblocks*	*When*	*Comments*
Telecom Datacom Equipment Telecom Datacom Infrastructure Cable Plant High Perf. Computing & Storage Digital Audio Special Apps	Package Types	Types	C,R,M	C,R,M	C,R,M	C,R,M	Cost vs. Cu*	2000s	Many styles avail. Cu-to-FO decisions based on specific FO advantages: bandwidth, crosstalk, security, distance. Future bodes increasing use in HPCC, Industrial and Commun. Markets.
	Fiber Types	Types	MM,SM	MM,SM	MM,SM	MM,SM	X-Linkages: Optical Si PWBs Design Tools Communications HPC FTTH	Below	
	Max. # Pins	Quantity	24	48	72	144		2014	
	Max. Wavelength	nm	850	1310				2016	
	Housing/Ferrule	Material	C,P,M	C,P,M	C,P,M	C		2009	
	Attenuation Range	db.	0.3-1.0	0.15-1.0	0.1-1.0	0.1-.8		1990s	
	Max. Operating Temp.	^{0}C	85					2000s	
	Max Circuit Speed	GHz	Essentially unlimited by SM Fiber					2000s	
	Alternative Technologies	Type		Advances in Cu Interconnect & Circuitry to ~40Gbps					
	Technical Issues	Type	End Face Prep, Assembly, Alignment, Attenuation						
	Supply Chain Issues	Type		Developing World Supply Issues. US Mfg. Support					
	Encroaching Technologies	Type		Cu Circuitry Improvements					
	Cost Issue	Type	Cu always cheaper, but cost/Gb will favor FO above 40Gbps, and post 2018-20 be the only solution for high performance data center applications. Cost will come down with volume						
Future SiPh Systems	Integration of Optical Si with PCB and chassis Level FO	About		New FO and Waveguide connectors may need to be defined. EOPCBs do not exist, will have to be developed or employed as fly-over cables. Terabit connector systems with acceptable economics are needed.					
Trends	Fiber Optics=multi-tiered technology. 1]Low cost LED/POF specialty applications in copiers, automotive, sensors, etc.; 2] telecom applications in the local, distribution loop, central office and long haul networks; 3] high speed LANs and SANs; 4] high performance electronic equipment interconnects. FTTP at from 30 to 100Mbps is in initial roll-out after decades of planning – beginning with Verizon and Bell South. FO future tied to success of broadband FO deployment + degree of UWB wireless competition to wired telecom. Massive investment over the past 2 decades in fiber optics R&D has produced a stable of technology that is yet to be fully realized in commercial application. EO is capable, albeit at 2 to 10X the cost of Cu, of satisfying any foreseeable roadblock related to speed or bandwidth, but will see only high end use in OEM equipment thru 2010-15. FO connectors tooled and available for production use include: ST, FC, LC, SC, FDDI, MT/RJ, MU, E2000/3000, and MT ferrule based MPO, MPX & others. POF remains a specialty. Connectorized transceivers are also available [GBIC/SFP]. ATM/Sonet frequencies from OC-3 [155Mb] to OC-192 [10Gb]. Fiber flex, ribbon fiber, free space and embedded optical trace technologies are also available when on-board optics is required, as are optical backplane interconnects – including hybrid Fiber-Cu devices/systems *Absolute cost vs. Cu often not a good measure of FO effectiveness. There are applications where cost comes into play. Example: Intel Lightpeak 10Gb bus. Cu can do the job at lower cost. But other apps, such as telecom and military would not be possible w/o fiber.								

C=Ceramic, P=Engineered Plastic, M=Metal C=Circular, R=Rectangular, M=Multi conductor, MM=Multimode, SM=Single mode, Ce=Ceramic, SAN=storage area network, FTTP=Fiber-To-The-Premise, POF=Plastic Optical Fiber, GBIC=Gigabit Interface Converter, SFP= Mini GBIC/Small Form Factor Package, ATM=Asynchronous Transfer Mode, Sonet=Synchronous Optical Network, HPCC=High Performance Computing & Communications.



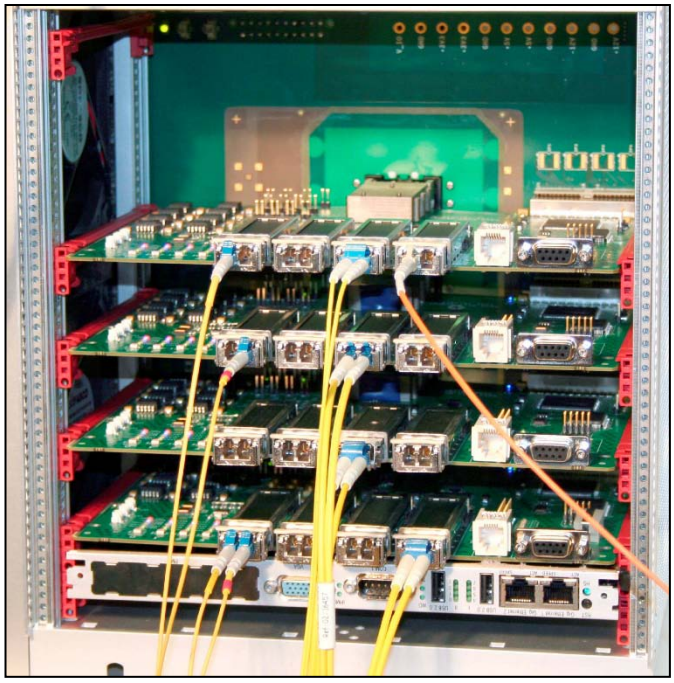
Molex Optical Backplane Connector System (LC)

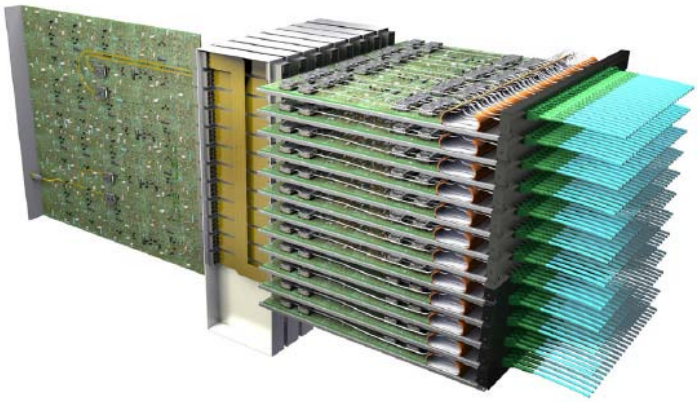


TE Connectivity Rugged 1.25mm Connector for Mil/Aero

Molex Optical Cables – above, left: Connector.com

Molex Illustration: Optical Card Cage for Storage App





TE Connectivity Passive Backplane

Methode FO Connectors clockwise FC, ST, SC, LC

2015-2025

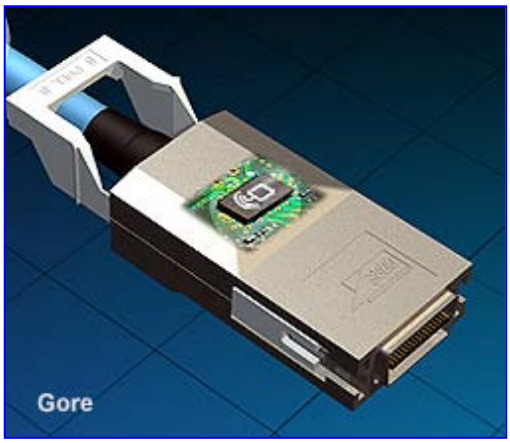
FO Connector developments will be closely tied to trends in OICs and equipment design. Within the timeframe of this roadmap, significant progress, if not breakthroughs will be made. The driving force for these developments will be in Si ICs, key system designs employing board level FO, and future advanced broadband communications and high performance computing.

Optical solutions will become the technology of choice at shorter and shorter distances as increased total data volumes drive up data rates, power consumption and cable count. Reduced cable bulk and weight are additional advantages of FO. Cu-based interconnection appears to be viable for backplane applications up to 20 Gb/s – but fixed Cu-to-FO active cable assemblies for 10 Gb Ethernet, InfiniBand and other high speed applications are now a reality:
TE Paralight^{tm} (r): 5-20 Gbps ⇨ 10-40 Gbps w/3.3v 50um fiber for 100+ meters.

FO

CONNECTOR TECHNOLOGY TRENDS:

The balance between copper and fiber has been slowly shifting over the past 10 years due to a number of factors. Prices for all types of fiber optic cables have declined while characteristics have been improved including reduced attenuation, greater durability, and resistance to damage from bending. Transceivers have also seen a major transformation as they have become more efficient, drawing less power, and packaged in smaller envelopes. The average bit error rates have also been improved.

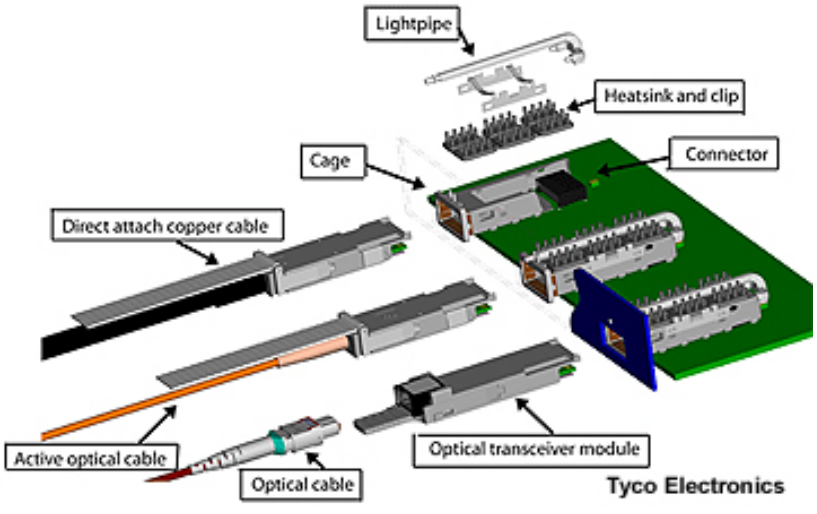


As data rates increase to multi-gigabit frequencies, it often becomes necessary to implement active signal conditioning features including equalization and pre-emphasis to compensate for losses and signal distortion generated by longer copper cable lengths. This requires the placement of active devices either on the PCB or on a paddleboard located within the strain relief of the cable assembly. All of these factors have added complexity and cost to the copper solution.

Changing the mindset of an industry that has relied on copper interconnections from its infancy takes time and years of successful experiences. Existing options offer some of the advantages of both copper and fiber interconnect and are proving to be very popular.

Small form factor pluggable modules such as SFP+ and QSFP+ consist of a common PCB header which accepts direct attach copper cables as well as an optical transceiver module. A fiber optic cable terminated in a standard connector plugs into the back of the transceiver module. This arrangement allows the equipment manufacturer to build their product using a standard I/O header while the user can choose either copper or fiber external links. A system can be easily converted from copper to fiber at any time in the future as needs dictate.

Another alternative is the use of an active optical cable assembly. Active optical cables are terminated at both ends with an industry standard copper interface such as the Infiniband connector.



Electro-optic transceivers are mounted on a small printed circuit board located within the strain relief at both ends of the assembly.

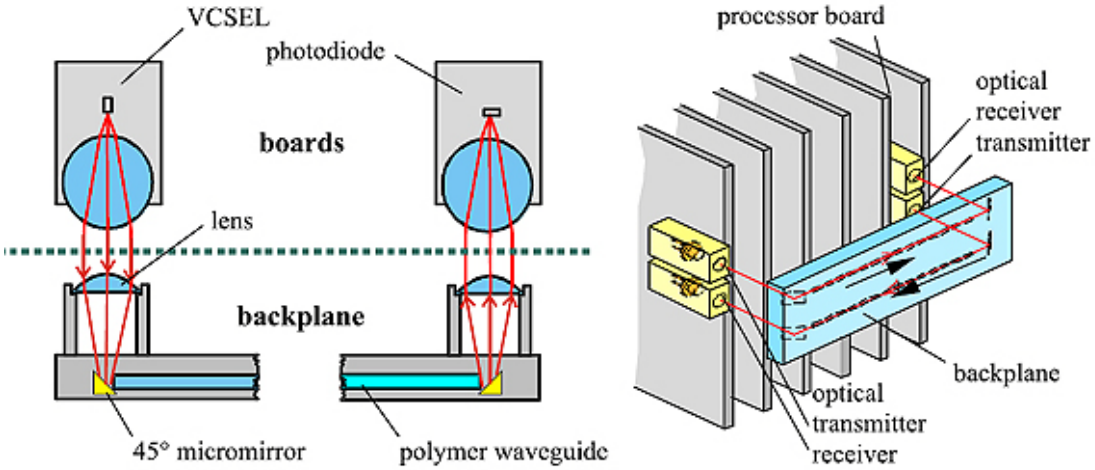
Power for the conversion process is drawn from pin G7 per the InfiniBand specification. A small diameter fiber optic cable exits the rear of the strain relief and links the two ends of the assembly.

The resulting active optical cable is a plug-and-play equivalent of a copper cable that can extend reach from 10 meters to 100 meters and possibly to 300 meters. The fiber optic link dramatically reduces cable weight and bulk, two very important factors in data centers and server farms that may require interconnect among thousands of rack-mounted boxes. Interest in the long term advantages of expanded bandwidth headroom are driving development of optic alternatives of common I/O interfaces. The objective is to provide a degree of "future proofing" to insure that the same interface will be capable of supporting future generations of equipment without changing the hardware. Universal Serial Bus (USB) connectors have become the defacto-standard in a huge variety of commercial, industrial and consumer applications. Over the years, its bandwidth has been increased to keep pace with the data rate demands of new equipment. The latest iteration, USB 3.0, has a theoretical bandwidth of 5 Gb/s, well in excess of most current applications.

Intel recently stepped beyond the USB 3.0 introduction to announce their LightPeak[tm] fiber optic communication technology. One 12 mm square chip does the electro-optical conversion with initial bandwidth of 10Gb/s. This optical interface provides plenty of bandwidth headroom as new applications emerge.

A simple four position optic connector provides a consumer friendly separable interface, and is remarkably similar to the shape and size of a USB connector. It has been suggested that Light Peak may be considered USB 4.0.

Optical Backplanes Interest in expanding the use of optical interconnects to the backplane generated extensive research in the late 1990's, but the 2000 to 2003 recession put much of this work on the back shelf. Several potential technologies including the use of laminated polymer optical waveguides embedded into a conventional backplane were explored.



The ability to tap this layer and direct an optical signal 90° up into a connector has been a difficult challenge.

A series of recent white papers indicate that development work on true optical backplanes is continuing as new technology becomes available.

Interest in fiber optic interconnects continues to grow in a variety of military, avionic, industrial control, and even consumer products. In March 2010 the VITA trade organization announced the formation of a study group to investigate fiber optic technology that enables high density optical interconnects in embedded systems. Within a week the U.S. Air Force researchers based at Wright-Patterson AFB issued a call to the industry to improve photonic interconnect manufacturing technology to speed adoption of fiber optic interconnects in military applications.

As indicated above, substantial forward-technology developments in Fiber Optics was lost as a result of the 2001-2003 recession, not just at the interconnect level, but in system architecture and design using free-space and polymer waveguide technology. Part of this loss was the result of vastly improved Cu interconnect systems, and part due to companies eschewing longer-term research projects.

Ways need to be found to achieve continuity in long-term research areas between government and industry. We estimate the previous recession and the implosion of the Dot Com bubble set back FO research by at least 10 years.

PRIORITIZED NEEDS:

OEM Buy-In to SiPh Systems Technology

Down "in the trenches" of the connector and PCB industries, they have learned not to venture far from stated needs of OEM customers. Ironically in SiPh there are undoubtedly programs in progress covered by NDAs, which prevent their discussion outside of that OEM or other application, such as a foreign country's photonic development programs. This program needs OEM buy-in to prioritize the roadmap in the component supplier's minds. Among those OEMs are: Intel, Cisco Systems, Microsoft, IBM, HP, Juniper, perhaps Dell, and others.

Collaboration and Input from the Interconnect Industries

This program's objective is to roadmap these technologies. To do so we have needed input from the connector and PCB industries, which is difficult due to a number of reasons: i) committed to NDAs, ii) committed to foreign programs of this nature, iii) No time for non-revenue generating activities in 2 industries decimated by offshoring, which in the case of connectors was of their own doing and of necessity, iv) were or are being acquired. Many thanks to those who did input, particularly TE Connectivity.

- Amphenol
- FCI
- Molex
- Samtec
- TE Connectivity
- US Conec
- Corning Glass
- MFLEX
- Calumet Electronics
- TTM Technologies/Via Systems
- ConnectorConsultants.com
- ConnectorIndustry.com

Specific Technology Input

There are specific applications that must evolve in our thinking on this project, including:

- Planning for Chip, Optical Alignment, Package and Board-Level Photonic Interconnect
- Need for and Solution to Embedded Waveguides
- Embedded Waveguide-to-Surface Layer Connector re: above
- SM Optical Interposers and Sockets
- SM Optical Transceivers $\geq$ 100-400Gbps
- Direct Chip-Attach Optical Interconnect (bypassing package overhead)
- Strategies on how to reduce costs in an already mature technology

TECHNOLOGY NEEDS

The connector industry, albeit limited to a few large domestic suppliers, has the technologic capabilities to meet future challenges posed by this program. One issue may be a need to launch into the semiconductor domain with MEMS-style capability for micro-interconnect alignment. Since knowledge of this capability is widely disseminated, there should not be a problem if this arises – as it has with optical ferrule technology. The industry is already using semiconductor VCSEL capabilities in active cable assemblies and board-level transceivers.

The printed circuit board industry on the other hand, is severely limited visa-vis domestic HVM production and supply chain. Adopting embedded optical fiber will be limited to a few domestic suppliers, but there would be several Japanese and Taiwanese suppliers who would entertain this capability. Most likely, embedded waveguides will emanate from IC packaging suppliers such as ASE or Amkor, within the domain on the Packaging TWG.

GAPS & SHOW-STOPPERS

Gaps and Show Stoppers for Interconnects exist primarily in being able to reduce cost 2:1 to 5:1 in relatively mature technologies. The industry would need HVM applications in the 100s of thousands to millions, with a stable market in order to automate these designs.

Interconnect Technology Hurdles are doable IF volume applications exist with OEM buy-in. However, there is a tendency by large OEMs to ‘own’ all technologies in their proprietary designs. This transcends any desire to keep the technology domestic and ‘open’

The biggest interconnect question mark has to do with the timing of transition from Cu signaling to Photonics at the Chip, Package and Board Level of Datacom and Computer/Server/Storage equipment. The IO port and $\leq$ 1km cabling are already covered. FO Backplane and Cable connectors already exist in both MM and SM designs. The key may be in 4 stages over the next 2 decades:

1. **2015-18:** Existing hodge-podge of proprietary, company-specific and standard interconnect designs, which do fulfill existing applications, if at a high cost. Existing Above Board Optical Fiber Interconnect, mostly MM with no Waveguides. Cu designs such as Intel’s OCA system for data center applications up to 100Gbps at 3m will continue and probably delay full implementation of fiber-based systems. This has been proven out over years of constant improvements in metallic circuitry, and there is no reason to expect otherwise.

2. **2018-20:** Evolution of Standards based on an interim Hybrid Approach to Photonic Chip Packaging, not too dissimilar than what exists today with InP Transceivers. First Use of SM in electronic packaging w/ discrete hybrid Transceivers. First Use of Embedded Waveguides with Peripheral Interconnect and SM Connectors and Cables.
3. **2020-25:** Heterogeneous SiPh solutions with advanced 3D Packaging. Embedded Waveguides w/Surface-Level Interconnects MM and some SM inside the box. Some of this will happen sooner.
4. **2025-35:** Monolithic Integration resulting in Single Chip or Complex 3D Chip Solutions with Minimal Outboard photonics Interconnect at the System Level. Interconnect will be Primarily Between Equipment and Networks. SM Optical Fiber and Waveguides will be used to IO port and beyond. There is evidence of Monolithic SiPh commercialized *before 2025.*

POTENTIAL ALTERNATIVE TECHNOLOGIES

1. **Free-Space Optical Interconnect** At the Backplane and
2. **Beyond Optical Fiber** Planar Waveguide Developments.
3. **'Brick' Systems** Composed of Devices, Waveguides and 3D Packaging with IO Ports to the Outside World, 1.e. 2025-35

IOT APPLICATIONS AND TRENDS

The Internet of Things will be an illusive subject, because many of its applications are at this time 'hoped for', extremely broad and disjointed. One common thread is where the data goes: to a Data Center to crunch the numbers and provide feedback and control. The cumulative effect of this: mountains of data. IoT proposes to use local sensors, feedback and internet-connections to monitor and control a 'global' range of electrical and electronic products:

- LED Lighting
- HVAC
- Appliances
- Consumer Electronics
- Industrial Equipment
- Heavy Machinery, Refining and Chemical Processes
- Banking and Vending Machines
- Retail POS and Back Office
- Shipping, Containerization, Inventory Control and Logistics
- Autos, Trucks and Buses
- Railroads
- Roads and Bridges
- Medical and Biomedical Devices
- Wearable Electronics

There will be Sensing and Communicating Modules – some photonic, and eventually Single Chip Solutions. Applications with high bandwidth, long distances and harsh environments will gravitate to

photonics. There is also a 'Wild Card' in existing and Internet II Cable TV and Internet Infrastructure, which will have to improve to GB and eventually TB speeds, requiring the latest in SM Optical Fiber (at least in) Backbone solutions (or be Wireless) to-from Internet providers, Micro-Satellites or Balloons. This will include the bandwidth demands of 4K and 5K HDTV, virtual reality and new services not yet invented.

There are few potential issues for Connectors here, and many/most low speed applications will be Cu or MM fiber at the network node and/or Low Cost/Flexible LED/POF Interconnect where the fiber can be cleaved with a razor blade. 802.11ac will play a major role as will Internet service-provider networks. The prime area of IoT interconnects will be as follows:

- SiPh and Cu Device Packaging & Micro-Interconnect
- Sensor Module IO incl. some with SiPh transceivers
- Premise/Network Cables and Wireless Access to Routers, Switches and Modems
- Smartphone-based Sensor Networks
- Optical/Coax NIDs
- Outside plant cable infrastructure

Mil/Aero applications are also in the mix for IoT, and this project will attempt to cover some of that in year 2. Mil/Aero will benefit from Commercial Equivalent cost reduction, potential dual-use, and their special applications will be enhanced by progress in this program. The domestic connector and global PCB industry are positioned to address these applications, although there are serious issues with domestic manufacturing since most high volume board assembly and system-builds have been outsourced to EMS suppliers in China and other Asia-Pacific regions. In Phase 2 we will entertain additional input from DARPA and DoD. IoT will tend to use mature technologies such as fiber optic connectors and cables, plus new technologies in the sensor area.

CONTRIBUTORS AND THOSE HAVING THE OPPORTUNITY TO MAKE INPUT

Editor's note: Many have accepted the roadmap as written or did not edit due to other priorities, which have focused the remaining domestic U.S. interconnect industry on today's business and supporting global marketing, development, and manufacturing sites. NDAs with OEM customers in this area of technology have also suppressed some input.

- John L MacWilliams TWG Chair, Principal, US Competitors LLC, consultant to connectorindustry.com and author of INEMI roadmaps since 2000.
- Bishop & Assoc. Connector Industry Support Organization - incl. Bob Hult's analyses
- TP Bowen, Optical Interconnect Fellow, TE Connectivity
- Mustafa Mohammed, DOW Corning
- APEX Electrical Connector Consultants – Chuck Blichasz
- Amphenol Intercon Systems – Dick Kauffman
- Roadmap Reviews to Molex, Samtec, FCI, 3M and others in the connector industry
- IPC 2015 Technology Roadmap
- Huawei Circuits, Dana Korf
- Celestica: Tatiana Berdinskikh
- INEMI, PSMC editing, Robert Pfahl
- TTM for the domestic PCB industry – Marika Immonem
- INEMI 2015 Connector Roadmap

ASSEMBLY AND TEST ROADMAP

Contents

ASSEMBLY AND TEST ROADMAP

EXECUTIVE SUMMARY

The overall cost, including especially the cost for assembly and test, of optical devices needs to be reduced substantially so that optical products are cost effective in more applications. Many of the most important potential applications require single mode technology where assembly of parts requires tolerances and stability of the optical chains over the lifetime of the product in the operating environment of less than 1 micron. Achieving that level of mechanical consistency requires starting with the design, selecting materials and structures to minimize the effect of temperature and stress and other environmental phenomena, selecting materials , joining methods, and assembly processes that will yield that result. Generally, materials with high modulus and low TCE are best and have been used extensively in optical devices. Unfortunately these materials tend to be expensive so much effort is devoted to utilizing lower cost materials and the lower cost processes.

Detailed mechanical and optical properties of the materials used in optical products are often not available. Standardizing on those materials and making the properties available will enable designers to model optical products better and minimize the need to build and test hardware.

An obvious way to avoid assembly cost is to minimize the number of parts to be assembled. That is being addressed through the increased use of integration. Unfortunately, all of the functions needed in optical applications cannot be integrated yet so assembly, or heterogeneous integration as it is often called, is needed.

Assembly methods and equipment from the microelectronics industry are often the initial choices considered for optical products. Many of these processes are perfectly suitable for optical devices, especially the electronic and non-dimensionally critical functions. In addition, a sub set of the electronic methods are effective for the high stability design and assembly methods. The chapter emphasizes the character of joining methods and highlights those standard processes, materials and equipment that are suitable for that demanding requirement. Thermocompression bonding, welding and UV cured polymers are often good choices.

Processes to achieve the 0.1 micron tolerances required for true passive alignment of optical devices are not widely available. Many approaches are being investigated to fulfill that need and avoid expensive (because it is slow and requires expensive equipment) active alignment where the optical chain is activated and used to actually ensure alignment is adequate.

A common request is for “equipment able to align parts to <0.1 micron of accuracy.” Equipment to achieve that level of accuracy is not yet readily available. What is available is equipment able to achieve 0.5 micron accuracy. That capability needs to be improved. To capitalize on the resulting equipment, other steps are needed; overall design, inclusion of fiducials and reference points, selection of stable joining methods and joining materials, etc. In addition, improved interfaces to equipment are needed. These interfaces must reduce programming, set-up and change over times to minimize the cost to build high mix low volume optical products.

Optical test is complicated by the need to provide not only optical sources and detectors but usually similar electronic functions as well. The 10 to 100 GHz speed of many optical devices requires expensive equipment. In addition, optical signals have many parameters that need to be both generated and measured; wavelength, power, modulation rate, modulation method,

polarization, etc., often for many channels simultaneously. 12 channels are common today with roadmaps forecasting over 1024 channels in the future. Providing all those sources and detectors results in complex, expensive test sets.

INTRODUCTION

The objective of this chapter is to roadmap heterogeneous integration assembly processes required to build Silicon Photonic Systems at minimum cost and highest reliability. Much of this work is groundbreaking, but to the extent possible we must enhance proven techniques, particularly imaging, passive alignment and state-of-art pick and place equipment to achieve cost/volume goals.

Nothing in this chapter signifies unbendable roadblocks, but dimensional challenges exist at the device, module, packaging and component levels

The inclusion of an assembly TWG acknowledges that in the foreseeable future we expect to build photonic products utilizing multiple parts, i.e. not totally integrated on Si chips and substrates.

The most demanding assembly issues arise with assemblies that will utilize single mode (SM), as opposed to multi-mode (MM), optical devices and technology. SM is likely to dominate because SM technology enables many functions that are not viable with MM. Specifically SM allows Mach-Zender modulators, gratings to filter and turn light beams, adiabatic tapers to minimize power loss, reach up to 100 Km with minimal dispersion and power loss, etc. In addition, data centers, the fastest current growing application, are moving toward SM technology which seems likely to be used for interconnect into the rack to at least the backplane and eventually on board.

To implement all of the capabilities that are physically possible with SM devices, parts in the optical chain must often, but not always, be aligned to within a fraction of the 0.65 to 1.6 micron wavelength of light that is typicallyused.. Thus these critical parts must be located with respect to one another to as little as 0.1 micron, not only during the assembly process but over the lifetime of the final device. The expected lifetimes are typically years in a variety of operational environments. Environments include temperature variations, mechanical shock and vibration and exposure to water and other potentially detrimental agents.

Another key objective is to reduce and minimize cost, which is both volume and process-dependent. Minimizing the number of parts to be assembled and simplifying the assembly processes required is critical to reducing the final product cost. While assembly is not free, in many photonic products, the cost of the parts, not assembly and test, dominates the total cost. Typically, the higher the levels of integration possible for a product, the lower the cost. However, ultra large scale integration (ULSI) requires very high volume to justify the up-front investment in the fabrication capability. In many cases islands of integration are more cost-effective than expensive fabrication capability.

SM devices have historically required active, tuned alignment during assembly. The cost of those processes are high due to the complexity of the equipment and slow assembly time. Thus low cost implies passive alignment in which parts are placed and fastened in place without using performance of the optical chain to determine that parts are adequately aligned. Thus much of the effort required to develop assembly processes revolve around achieving that objective.

Traditionally, test of photonic products has been done at the end of the manufacturing process and, with the exception of active alignment, minimal testing is done during manufacturing. On

the other hand, much design verification and qualification testing is traditionally done before production began. The first photonic data communications product were built by the Bell system to their standards which were very demanding, required up to a projected 40 year life and were thus fabricated utilizing robust, usually hermetic metal, glass and ceramic packaging. Applications today will not support the resulting high cost, do not require such long life and are built utilizing lower performance technology.

Finally, the overall system level assembly process consists of 3 main steps:

1. Addressing assembly and test issues when designing the product.
2. Bringing together the parts to be assembled and locating them properly with respect to one another.
3. Forming permanent joints between parts that will provide suitable joints for the life of the product.

SITUATION (INFRASTRUCTURE) ANALYSIS

DESIGN REQUIREMENTS

Low cost, high performance optical products start with good design.
Good design for optical devices requires:

- Minimizing the number of parts
- Choosing parts that are adequate but not overly specified
- Minimizing the number of assembly steps
- Utilizing massively parallel fabrication and assembly methods such as wafer fabrication, die-to wafer bonding or even wafer to wafer bonding rather than part-by-part placement and joining
- Understanding details of parts and working with manufacturers to ensure the parts chosen have:
    - the necessary dimensional consistency
    - suitable location reference points
    - surfaces to which suitable joints can be made
    - shipping package containers that interface with manufacturing assembly equipment (i.e. in tape and reel, waffle pack, etc.)
- Evaluating the extremes of part specifications and dimensional tolerances to ensure the design will be robust
- Maximizing the tolerances required as best as possible
- Ensuring that dimensional requirements can be achieved by ensuring that:
    - fiducials and other reference points are adequate for the tolerances desired
    - joining methods and materials are compatible with the dimensional and tolerance requirements
    - suitable manufacturing equipment is available to assemble the parts

A specific and important design parameter for optical products, especially those utilizing SM technology, is evaluation of the dimensional variations inherent in both the assembly process and the operating environment over the life of the product. Maintaining location consistency of 0.1 micron for optical chains that often have dimensions of 10 mm, or so, requires avoiding movement due to mechanical stress, temperature changes, temperature gradients, aging, cold flow and other phenomena. This implies avoiding changes in the optical chain greater than the 0.1 micron required over the 10 mm, or 1 part in 100,000. (That is equivalent to 1 mm over 100 meters, a distance a little longer than an American football field.)

Achieving this degree of stability requires consideration of the properties of the materials (thermal expansion coefficient differences, the modulus of the materials, material strength, Poisson's ratio, etc.), and assembly process temperatures of 85 C to as high as 250 C, environmental stress testing from -40C to +125, shock to 1000 gs, etc. The behavior of materials under these conditions is governed by the Generalized Hooke's Law listed in Appendix B.

These equations relate Young's modulus, Poisson's ratio, Temperature and the thermal coefficient of expansion, to stress and strain. These equations imply several important things:

1. When temperature changes, something moves OR the stress increases at a rate established by the coefficient of expansion and Young's modulus.
2. When something is stretched or bends, thus changing strain, stress increases in accordance with Young's modulus.
3. A higher Young's modulus implies less motion with strain or temperature changes.

These generalizations are of limited value but make the point that achieving stable, accurate known dimensions through the manufacturing process and environmental stress over the life of a product requires taking into account these detailed material properties.

One result of these issues is the need and benefit from using high modulus materials such as ceramic, glass and metal, ideally with low thermal expansion coefficients. These high modulus materials minimize relative part movement under stress and temperatures changes, are not as susceptible to property changes and corrosion from exposure to the environment and do not exhibit major phase changes in the manufacturing and use temperature ranges, all of which are minimize mechanical movement. Another benefit of these materials is that they often provide a sealed hermetic environment that minimizes

Generalized Hooke's Law

Appendix B describes the behavior of materials when they are stressed, strained, or their temperature changes. These equations and their implications drive the deformations and shape changes that occur in material and combinations of materials due to temperature and stress or strain changes. While they may look complex, they are relatively simple. For example, when the temperature of a material changes the length of that material changes due to TCE, or, if the material is constrained in 1 or 2 dimensions and cannot move freely, the stress will change with Young's modulus and the material shape will change in the unconstrained dimensions by an amount set by Poisson's ratio. In more generalized combinations of conditions, the equations describe bending, shear stresses, etc., and can be used to predict motion that exceeds the elastic limit resulting in failure or permanent deformation, for example.

environmental effects. As a result, this technology is referred to as hermetic packaging.

Unfortunately hermetic packaging tends to be expensive. Thus engineers are moving to lower cost materials and methods that usually incorporate organic materials. The organics have lower modulus and thus move more with stress, have higher coefficients of expansion (up to 10X) and thus move more with temperature changes, and lower thermal conductivity leading to temperature gradients that induce stress and hence movement. The resulting shape changes are often not simply an increase in X, Y or Z but some complex mix resulting in warping, "saucering" or "potato chipping".

One of the more demanding mechanical requirements is maintaining planarity especially due to the requirement that modern electronic products be "thin" meaning a few mm thick. Parts about a millimeter thick are not inherently stiff and easily become non-planar if larger than few centimeters. This is an important issue in reflow soldering of micro ball grid arrays for example.

Assembly processes often introduce materials to form joints between parts; epoxies, solders, adhesives, etc. The properties of these materials are as important to dimensional stability as the properties of the basic parts. This issue is addressed further in a later section and table of joining methods.

In summary, these phenomena make holding dimensions in products to 1 part in 100,000 challenging.

The use of finite element analysis can often elucidate these changes and enable the engineer to make suitable choices. (See Appendix B)

The critical questions to ask related to assembly before the design is finalized are:

- Are the locations on parts that need to be accurately located with respect to one another well defined by features the equipment can use as a reference?
- Is the assembly equipment able to find the location of these critical points on the parts to be assembled?
- Is the equipment able to move the parts into position with respect to one another with the needed accuracy?
- If joining materials are used, will they adhere to the part surfaces?
- Are the surfaces to be joined close enough to be joined?
- Will the joining temperatures and thermal profile distort the joint irreparably?
- Will all of the materials survive the assembly and operational environments and retain the desired location tolerances, especially during thermal cycling?

PARTS TO BE ASSEMBLED

Optical devices are likely to utilize the following parts that will be assembled utilizing the joining methods and equipment noted above.

- Passive optical components
    - Lenses
    - Mirrors
    - Isolators
    - Optical connectors
    - Fiber, both SM and MM.
        - Single fibers
        - Ribbon fiber: i.e.4, 8, 12, 16 …etc. fibers
    - Planar waveguide Structures with
        - Embedded waveguides
        - Gratings
        - Multiplexers
        - De-multiplexers

- Active Optical devices
    - Lasers
    - Photodetectors
        - PIN diodes
        - Avalanche diodes
    - Mach Zenders or other modulators

- Electronic devices
    - Electrical connections and connectors
    - Semiconductor chips
    - Passive components such as resistors, capacitors, etc.

These components are assembled on a variety of substrates or platforms including the following:

- Conventional FR-4 or FR-5 Circuit boards
- High Frequency Circuit boards using Rodgers 4300 dielectric for example
- Glass substrates with waveguides, optical vias, gratings and other features
- Silicon substrate with TSVs, electrical traces, optical waveguides, optical vias, gratings, possibly some active components such as detectors, etc.

These parts are assembled using a variety of assembly and joining methods as described in the following sections.

THE ASSEMBLY PROCESS

The main manufacturing processes for optical device are:

- Conventional surface mount assembly technology utilizing pick and place and reflow soldering when the results are suitable for the application.
- High accuracy placement and fastening utilizing suitable or specialized equipment and fastening processes equipment.
    - Laser welding
    - UV cured adhesives
    - Snap cured epoxies
    - Thermo-compression bonding
    - Brazing or soldering utilizing metallurgy that rapidly becomes rigid without cooling
- Flip chip assembly
- Wire bonding
- Dispensing of organic adhesives, encapsulants, underfills and adhesives
- Dispensing of optical joining materials such as UV cured adhesives that have good optical properties
- Assembly in particle free environments to minimize light scattering in applications where high contrast is important or where a particle will block light from micron sized pixels
- Testing utilizing suitable methods to inject optical signals and/or detect them

Optical processes differ from the related and widely adopted electronic methods in two ways;

- Some joints require greater accuracy as noted elsewhere
- Optical components sometimes require assembly in the third, or Z, dimension whereas most electronic assembly is on a planar surface. Thus, electronic equipment is not highly suitable for that assembly need.

Assembly that results in parts being joined together permanently is accomplished in two steps:

1. Parts are brought together and placed in the proper location with respect to one another, usually by machinery.
2. Parts are joined utilizing a joining method such as solder, epoxy, welding, etc.

BGA, MicroBGA/Chip-Scale self-alignment assembly techniques may be particularly useful as they are well advanced and in mass production.

The alignment of parts with respect to one another can be no better than the tolerance and uncertainty of the points of reference accessed by the assembly equipment. Reference points in the form of fiducials, well defined edges, etc. are critical to high accuracy assembly.

Traditionally many optical products were built in small volume and assembled manually. That is changing as optical devices proliferate and are built in higher volume. Thus, the following sections tend to address low cost automated methods.

Much equipment used to assemble and test optical devices is adopted from conventional electronic and microelectronic assembly and test equipment. While many of the optical assembly processes can be accomplished with this adopted equipment, the capability of existing electronic equipment that is suitable for the submicron tolerance processes required for some optical assembly is limited and in some cases inadequate. Thus specialized equipment for specific optical assembly process has been developed, often by adopting electronic equipment or, when necessary, developing specialized machinery.

Historically, specialized processes were developed to achieve the sub-micron tolerances required for aligning single mode lasers to optical fibers or other optical ports. Laser welding, for example, was developed and is used extensively as an assembly method. Parts are brought together. Heat, usually from a laser beam, makes the weld or multiple welds as needed. The needed alignment is typically achieved "actively" meaning the optical chain is activated and the quality of the alignment is measured by evaluating the output, usually the optical power, of the optical chain. By understanding the geometry and material properties, additional laser welds can be used to provide micro movement of components with respect to one another to maximize the desired output signal. This process is sometimes referred to as "laser hammering".

The disadvantage of this process is that the optical chain must be powered and the output signal detected while the parts are in the laser welder. That makes the equipment complex and expensive. In addition, the process tends to be slow, often requiring minutes per device due to the need to await temperature stabilization. The cycle time is lengthened further by the need to manually load parts, ensure the optical and electrical connections are made and then to go through the preliminary steps to provide macro alignment before the welding process begins. Once that is accomplished the second phase requires laser hammering to finalize the alignment. Thus, an important objective for manufacturing equipment is to avoid active alignment. Achieving that is essential to reducing cost. Hence much of the process engineering effort addresses that issue.

The critical questions to ask before the assembly process is finalized follow. These questions are similar, but broader, than those:

- Are the locations on parts that need to be accurately located with respect to one another well defined by features the equipment can use as a reference ?
- Is the assembly equipment able to find the location of these critical points on the parts to be assembled ?
- Is the equipment able to move the parts into position with respect to one another with the needed accuracy ?
- If joining materials are used, will they adhere to the part surfaces ?
- Are the surfaces to be joined close enough to be joined ?
- Will the joining temperatures and thermal profile distort the joint irreparably?

- Will all of the materials survive the assembly and operational environments and retain the desired location tolerances, especially during thermal cycling?

HIGH ACCURACY SUB-MICRON, LOW COST JOINING METHODS

Processes to achieve <0.1 micron alignment are not generally available. Processes, including the geometries, materials, joining methods and equipment to implement higher accuracy assembly are needed and under development. Methods being explored include the use of capillary action to move small parts into position, the use of silicon optical benches, i.e. silicon substrates with features such as "stops" and barrier fabricated as required to sub-micron location tolerances that serve as physical stops and thus act as locators.

As noted above, a very important need to reduce cost of optical devices, especially single mode devices, is to eliminate active optical alignment. Thus an emphasis on that need is inherent in much that follows. Specifically, emerging optical devices that utilize Single Mode technology require high accuracy (<0.1 microns) and low cost (implying a few seconds of time on equipment) joining methods.

Standard joining methods capable of fulfilling this high accuracy need are:

1. Metal deformation bonding
2. Non - Eutectic bonding with AuSi, AuSn, Cu Sn or other similar metallurgies.
3. UV cured polymers such as acrylates
4. Spot or laser welding
5. Si to Si bonding
6. New processes under development or to be developed

The following sections expand on these methods.

METAL DEFORMATION BONDING

If two clean metal surfaces are put in contact with one another and then deformed so as to at least double the area of the surfaces that touch, many metal combinations will bond and form a strong intermetallic joint. Some combinations of metals require higher temperatures, scrubbing of the surfaces mechanically or ultrasonically, or a controlled environment, usually meaning excluding oxygen. While the most common use of this technology in electronics is wire bonding[1], the processes can be used for other types of joints. This basic technology has the important advantage that it is fast; wire bond joints can be made at rates greater than 10 per second.

The following table provides details of some of these common processes that are used for wire bonding. While the table is specific to wire bonding, these same physical processes will work with other types of parts and provide the strength and speed needed for optical devices.

[1] George Harmon, "Wire Bonding in Microelectronics, Materials, Processes, Reliability and Yield", Second Edition, 1997, San Francisco, California, McGraw Hill, Page 148, Table I-6

Unfortunately, equipment to implement that type of bonding in optical devices is not readily available but could be developed.

Process	Temperature	Pressure	Common metal combinations		Environment
Ultrasonic wire bonding	20 C	yes	Al to Ag, Al to Au		air
Thermosonic wire bonding	150 C	yes	Au to Al, Au to Au, Cu to Cu	120KHz ultrasonic scrubbing	Air. At least N2 for Cu to Cu, forming gas preferred
Thermo-compression bonding	150 C	~ 20 gms per 500 sq. microns	Au to Au		Air but often aided by N2 or forming gas

NON-EUTECTIC BONDING

Some alloy systems have the interesting characteristic that when the 2 metals are heated in contact with one another to temperatures well below their individual melting points, they will diffuse into one another and form an alloy. The Au + Sn, Au + Si and Cu + Sn systems all have this property. These metallurgies can be implemented for use as a joining method by a., making parts out of the two materials, b., depositing these metals on the surface of parts to be joined using electroplating, sputtering or alternate deposition means c., utilizing a preform of one of the metals and then bringing them together and joining the parts with suitable pressure, temperature and gaseous environment if needed. After the joining process is completed, the remelt temperature of the new alloy is greater than the joining temperature resulting in a rigid joint that is formed quickly. This process stabilizes the joint.

UV CURED POLYMERS SUCH AS ACRYLATES

These materials are widely used in optical devices because the process is fast, the materials are transparent to a broad range of wavelengths, and are relatively easy to use. These materials can also be cured further with heat. Thus, a common practice is to "tack" parts in place with a "dab" of acrylate, expose it to enough UV to make a temporary joint, then remove this sub assembly from the primary joining equipment and complete curing the acrylate with more UV or heat.

One consideration and potential limitation is that common to many polymers. Young's modulus is relatively low and the TCE of the cured materials is relatively high implying that the material will move a relatively large amount with temperature changes or stress compared to metals and ceramics. These phenomena must be taken into account during the design stage.

SPOT OR LASER WELDING

Welded joints are formed by bring two pieces of metal into contact and heating them hot enough so that at least one, and preferably both, pieces of metal melt, flow together, and then cool to form an intermetallic joint.

Welding usually provides highly accurate positioning because the parts can usually be held in the desired location with respect to one another during the entire heat, melt, cool, solidify process.

Welding methods include spot welding, seam welding and butt welding, all of which use high current introduced to the parts to be welded using heavy electrodes.

Another method of introducing heat is with a laser beam. This can be a highly controlled highly accurate process but requires more expensive equipment than high current resistance welding methods.

An issue for high accuracy welded joints is motion during cooling. Welding requires exceeding the melting point of the metal which varies, of course, but often ~1000 ^{o}C. Motion can take place before the liquid metals solidify and then during cooling from the melting point to room temperature. Avoiding these motions requires good joint design and fixtures.

DIRECT WAFER BONDING

The following *in italics* is from the Ziptronics web site. It is reproduced here as it provides a good overview of this unique technology. While Ziptronics presents the technology for wafer-to wafer and die-to-wafer bonding, the technology may be useful more broadly.

DBI combines a room or low temperature, non-adhesive covalent bonding technique with integrated high-density interconnect formation. DBI makes possible 3D circuits and tiled wafers with the highest performance and lowest cost available, for silicon, III-V or other materials. Unlike other 3D fabrication methods, no wire bonding, solder bumping or pressure are required, and through-silicon vias eliminate large-area design exclusions.

DBI begins with chemical-mechanical polishing (CMP) to planarize the surfaces of the materials to be bonded. The CMP also exposes the respective buried interconnect connection points, or Through Silicon Via (TSV). Following CMP, a thin layer of silicon oxide (SiO2) is applied to both surfaces, which are aligned so the Supercontacts points will meet. The oxide is activated to create a direct spontaneous covalent bond formation. It exceeds the fracture strength of the bonded materials.

The bond energy between the surfaces is very high and brings the Through Silicon Via (TSV) into contact close to each other to form effective electrical connections.
Their low resistance enables better power efficiency and reduces the overall power consumption of the 3D system. Because the process is completed at room or low temperature, there are no residual stresses, such as can occur with thermal or anodic bonding methods, nor are there epoxies or other materials that require curing. The bond also is hermetic.

Material Preparation Requirements

- *Semi-standard waviness, bow and warp*
- *Inert RIE to clean surfaces and enhance surface porosity*
- *NH_4OH exposure terminates surface with amine groups*
- *Bond energies > 1 J/m2 obtainable at room temperature*
- *Oxide deposition + CMP to 0.5nm RMS spec*

The spectrum of possibilities includes combinations from silicon-to-silicon, germanium, indium phosphide, gallium arsenide, gallium nitride, quartz, and others. The resulting bond strength typically exceeds the fracture strength of the bonded bulk materials.

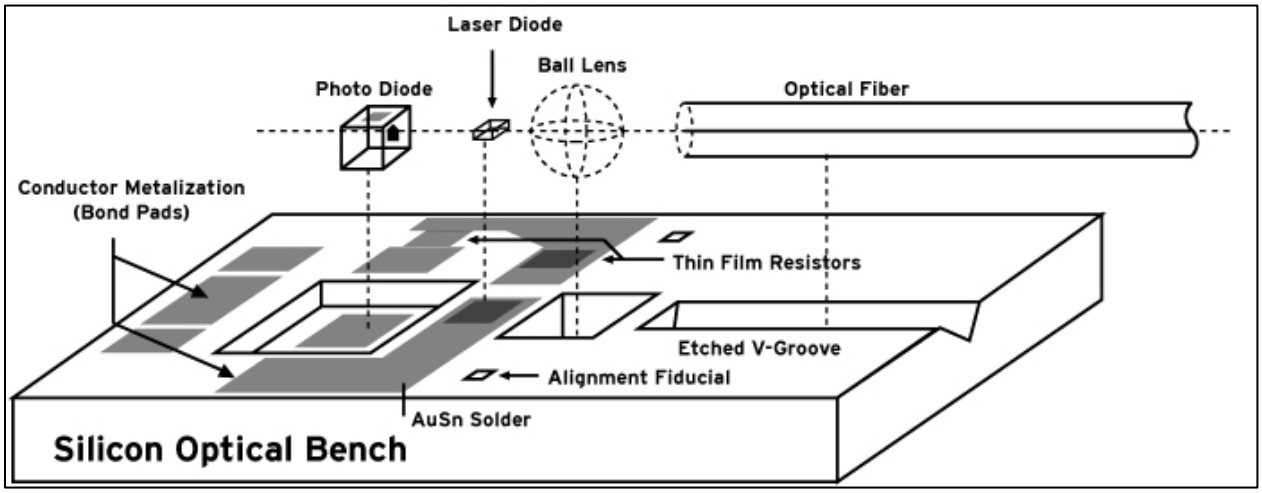
OPTICAL SPECIFIC ASSEMBLY METHODS: THE SILICON OPTICAL BENCH

This part fabrication concept was developed as a method to fill some high accuracy optical location requirements. The two figures directly below show such a structure and some of the features that the optical bench concept enables. The optical bench concept depends heavily on a phenomena characteristic of <100> silicon wafers. [2]Specifically, some single crystal materials, including silicon, have etching rates dependent on the crystallographic orientation of the substrate. This is known as anisotropic etching. One of the most common examples is the etching of silicon in KOH (potassium hydroxide), where Si <111> planes etch approximately 100 times slower than other planes. Therefore, etching a rectangular hole in a (100)-Si wafer results in a pyramid shaped etch pit with 54.7° walls, instead of a hole with curved sidewalls as with isotropic etching.

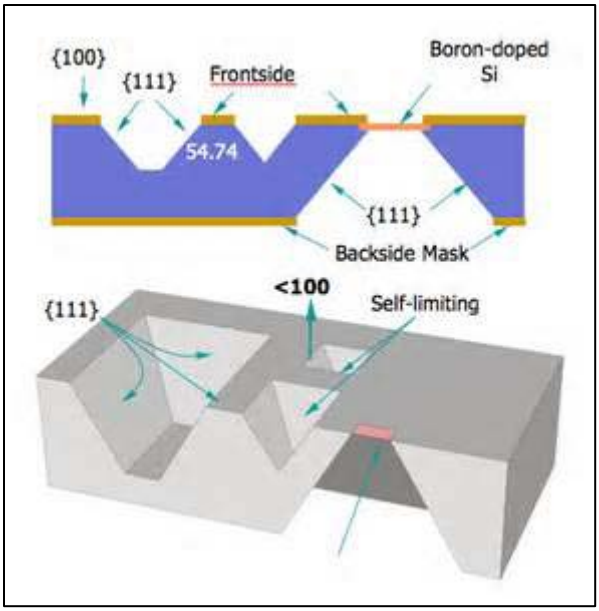
The technique enables the fabrication of a variety of features with highly accurate locations because their locations are determined by semiconductor lithography. This example shows:

- "V" groove for location a fiber made with a long, rectangular aperture
- Square pyramid pit for locating a ball lens made with a square aperture
- Larger pit for a photo diode larger square aperture etch to a stop
- Conventional electrical conductors
- Potential attachment methods.

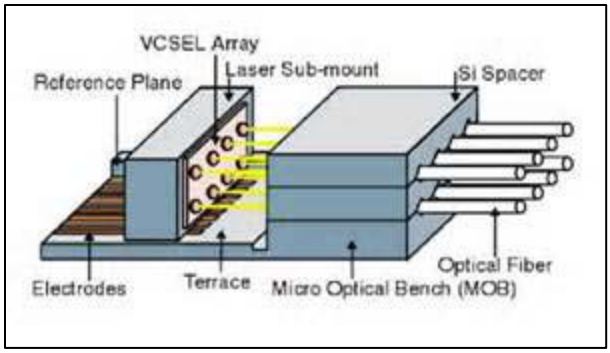
Utilization of the basic selective etch sensitivity allows many highly accurate structures to be fabricated.
[3]

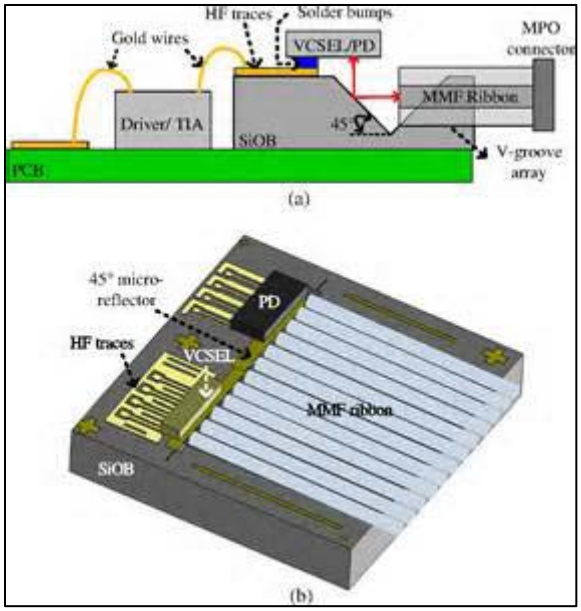


[2] From Wikipedia with paraphrasing.
[3] From Microsoft on line graphics



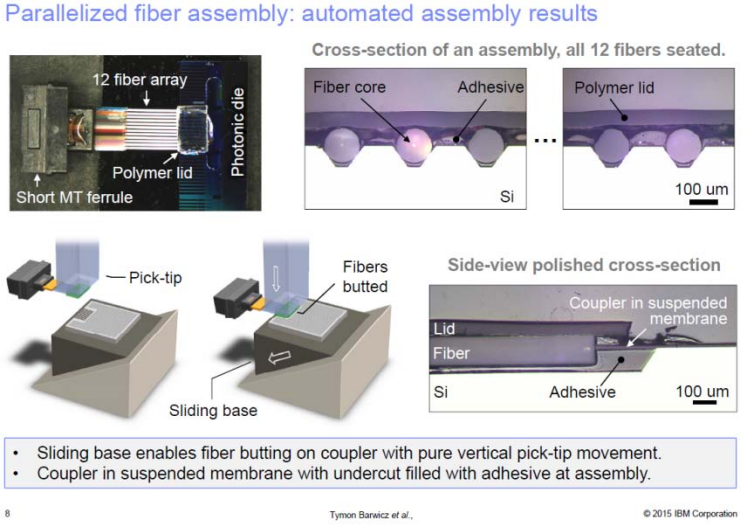
The next few figures illustrate some of the configurations that have been constructed utilizing this optical bench concept. These configurations usually incorporate more conventional assembly methods to complete the assembly process.





Fiber Alignment Utilizing Mechanical Fiber Butting & Capillary Action

A recent paper by IBM researchers described a method of aligning fibers accurately utilizing capillary action as illustrated in the figure below from that talk given to the MIT CTR in April of 2015. This method is potentially important, especially if it is combined with capillary action to assist movement of the elements into position and hold them there while the joining method is affected by cooling of a solder, solidification of an epoxy or UV curing of an adhesive. [4]



Optical fiber splicing

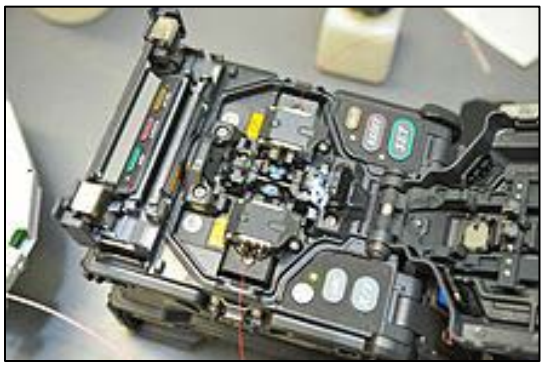
Fusion splicing was developed specifically to join optical fibers. Fusion splicers use an electric arc to weld two optical fibers together. The fusion splicing process uses localized heat to melt or fuse the ends of two optical fibers together. The process begins by preparing each fiber end for fusion. All protective coatings must be removed from the ends of each fiber. The fiber is then cleaved using the score-and-break method, usually with the aid of a tool or fixture. The quality of each fiber end is inspected using a microscope. The post joining attenuation of the fused joint is a direct function of the angles and quality of the two fiber-end faces.

The basic fusion-splicing apparatus consists of two fixtures on which the fibers are mounted with two electrodes. An inspection microscope assists in the placement of the prepared fiber ends into a fusion-splicing apparatus. The fibers are placed into the apparatus, aligned, and then fused together. Fusion-splicing usually utilizes electric arcs to heat the fiber ends causing them to fuse together. Arc fusion splicers can splice single fibers or 12- and 24-fiber-count ribbon fibers at the same time. The small size of the fusion splice and the development of automated fusion-splicing machines have made electric arc fusion one of the most popular splicing techniques in commercial applications. The splices offer sophisticated, computer-controlled alignment of fiber-optic cables to achieve losses as low as 0.02 dB.

[4] From an IBM Presentation to the MIT CTR in April of 2015. "Photonic Packaging in High-Throughput Microelectronic Assembly Lines for Cost-Efficiency and Scalability" Presented by *T. Barwic.* Authored by*T. Barwicz, Y. Taira, T. W. Lichoulas, N. Boyer, H. Numata, Y. Martin, J.-W. Nah,S. Takenobu, A. Janta-Polczynski, E. L. Kimbrell, R. Leidy, M. Khater, S. Kamlapurkar,S. Engelmann, Y. A. Vlasov, P. Fortier*

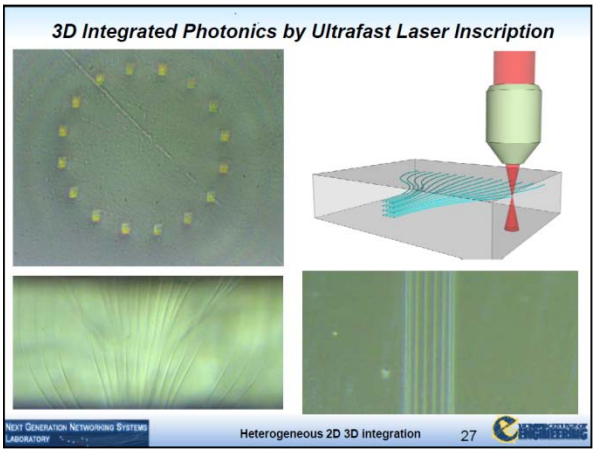
The picture to the right illustrates a conventional splicer.

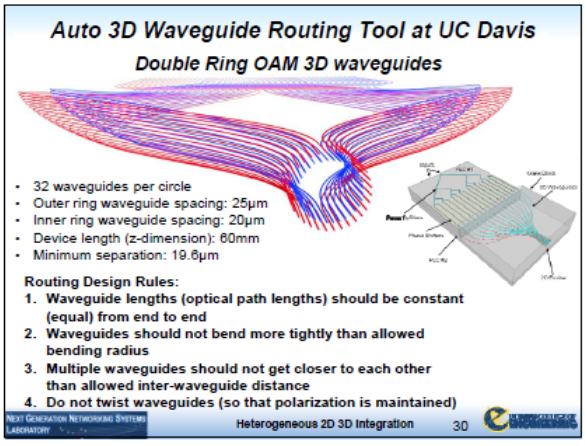
The detailed photo shows the actual splicing platform. The red fibers being spliced can be seen coming into and leaving the splicing point.



Laser Waveguide Formation

The graphics below are from the Yoo group at the University of California at Davis. This graphic illustrates inscribing waveguides within a bulk solid utilizing femtosecond laser pulses. Through the use of fiducials, cameras, high accuracy stages, careful measurement of parts and some complex software, waveguides can be accurately located within a bulk solid and used to fabricate a waveguide from one known point to another. Alternately, the process can be used to fabricate waveguide structures that are difficult to make utilizing other methods. For example, a structure such as a linear to circular transition can easily be fabricated.





The process works because the laser pulses increase the index of refraction enough to make a waveguide. An inscription rate of 150 mm/sec. has been demonstrated making the process potentially cost effective.

MATERIALS USED IN JOINING PROCESSES

The table following lists standard joining materials and methods used in optical products. Most of these are widely known and commonly used in electronic assembly including the electronics associated with photonic products. For electronic joining applications, the long term performance of these methods is generally adequate.

However, when the parts or elements to be joined must remain in place to submicron dimensions over the life of the product, only a sub-set of these methods will suffice. In addition, for some of the methods, the methods will provide the stability needed only if the joining material, such as an epoxy, is thin and has a high modulus. In other cases the method is simply not suitable for a joint that must be highly stable. In the table below, the color and comments delineate the suitability of each process and comment on its properties.

Primary Methods Used To Join Optical and Electronic Parts				
Color code Meaning	Suitable for sub-micron stable joints	Suitable for sub-micron joints if the stress is low and the joining material, if any, is thin, meaning less than a few microns.		Not suitable for sub-micron joints
Attach Material	**Application Methods**	**Thickness**	**Maximum Temperature**	**Comments**
Low Modulus Organic Joining Materials				
Epoxies, non-conductive electrically, low thermal conductivity	Needle dispense, stamp, dip part, Die attach Film (DAF)	5 microns and up	80 C - 200 C	Epoxies are the most common attach material used. DAF is applied to wafers before sawing.
Epoxy, thermally conductive	Dispense, stamp, dip, DAF	5 microns and up	80 C - 200 C	Conductivity <40W/m- ^{o}C
Epoxy, electrically conductive	Dispense, stamp, dip, DAF	5 microns and up	80 C - 200 C	
Acrylate Polymer	Dispense, stamp	>25 microns	80 C - 200 C 20C – 80 C	UV cured, non-conductive, good optical properties
Metallic Joining Materials				
Sn 63 Solder	Paste, preform, spheres, electroplate	25 to 75 microns	195C - 210C	Cold flows at 20 C.
SAC alloys	Paste, preform, spheres	25 to 75 microns	240C	Alloys of SnAgCu. SAC305 is 3% Ag, 0.5% Cu, balance Sn. Many alloys used. Generally high modulus. No cold flow.
$Au_{80}Sn_{20}$	AuSn preform, clamp & heat	~75 microns	280C	Typically utilizes a preform. Once alloyed with a little extra gold, the melting point is higher.
$Au_{98}Si_2$	Scrub silicon die, press and heat	<25 microns	280C	Requires scrubbing and pressure at temperature. Hard

				to achieve accurate location without complex automatic equipment.
Au thermo-compression	Gold to gold with pressure at temperature	< 100 microns	>150C	Requires > 20 grams of force per 2,000 sq. microns of area on EVERY joint. Not a strong joint.
Au thermo-sonic	Pressure with 120KHz ultrasonic	NA	>120C	Used for ball and wedge wirebonding.

Al ultrasonic		NA	20C	Used for wedge wirebonding
Braze	Reflow, controlled atmosphere	varies	650C	Typically done in a belt oven to join metalized ceramic and metal. Very stable joints.
Weld, laser	Spot or scanned beam	none	1000+ C	Brief temperature excursion in a limited area
Weld, electrical	Spot or dual pinching electrodes	none	1000+ C	Metal-to-metal in an engineered process to control part temperatures. Warpage possible.

While optical devices utilize many conventional materials, they also utilize specialized materials for specific applications. The most important differences relates to dimensional stability and maintenance of optical properties, particularly clarity, over the life of the product.

Materials with low modulus are inherently "unstable" dimensionally as stress from either temperature changes or external forces results in movement. Thus optical joining materials intended to hold parts in place tend to have high modulus.

Materials that yellow with age need to be excluded. Classic Sn63 solder cold flows under stress, moving to relieve the stress. That highly desirable property in electronic assembly is detrimental in high tolerance optical assemblies. The SAC alloys, for example, that do not cold flow, are a better choice for joints that must be stable.

Joining utilizing AuSn and CuSn is suitable for optical devices as these two systems form an alloy upon heating that is a solid above the temperature required to form the alloy. Thus, over these temperatures, the material is a solid and able to hold parts in position. The important point with these alloys is to ensure that when they reach the "activation" temperature, that the parts are located in the desired position and that the formation of the solid rigid alloy does not cause movement.

Material Properties Needed

An issue with some materials, especially organics, is finding their properties. Manufactures of materials often provide data sheets and by law must provide Material Safety Data Sheets (MSDS) that address hazardous properties. Unfortunately, the data sheets often exclude many of the properties that are important in optical design. Organics and silicones are often compounded utilizing a mixture of constituents to achieve a desired set of properties. Data on the properties of many materials is inadequate for detailed optomechanical design. Properties that are often needed include Young's modulus vs temperature, both before and after curing, CTE vs temperature, Poisson's ratio, dimensional change from water absorption and related % weight gain, dielectric constant and loss tangent vs temperature and frequency up to 100GHz, etc. The Industry needs standard sets of desired material properties developed and manufacturers to then routinely provide that data.

Epoxy joint Considerations

Basic Considerations:
In choosing an epoxy for a specific joint, the designer and process engineer need to consider the following points:

- Can the joint be designed so that it will meet the joint requirements when an epoxy is used as the joining material ?
- Does the epoxy need to be electrically, thermally conductive or non-conductive ?
- What modulus must the cured epoxy exhibit?
- Will the epoxy perform as needed in the post deposition manufacturing and operating temperature environment and will the epoxy negatively impact overall product reliability?
- How thick should the epoxy bond line be?
- How should the surfaces to be joined be prepared?
- How should the epoxy be placed on the surfaces?
    - Manual needle dispensed in a pattern?
    - Machine dispensed by needle or auger?
    - Deposited on one surface by stamping?

  - Film on part?
  - Preform?
- What % of voids is allowable in the finished joint?
- What viscosity is needed during deposition or during curing?
- What time-temperature profile is needed to cure the epoxy?

ACCURACY OF LOCATION WITH EPOXIES

Epoxies shrink during curing by varied amounts. That is a highly inconvenient property for high accuracy joining. The simplest motion is shrinking of a thin layer of epoxy used to hold 2 parts together. That can be measured and possibly accommodated.

A more difficult case is that where fillets are made using epoxy. When a fillet around a part shrinks, the shrinkage tends to pull the parts toward the shrinking material. If fillets are formed on four sides of a die, for example, the die can be pulled in 4 directions resulting in movement in the direction with the greatest "pull".

Epoxies also have a relatively high TCE; from 10 to 120 often 30 to 50 ppm/^{o}C. Above the glass transition temperature, which varies from -10^{o}C to +240^{o}C but is typically 85^{o}C, the TCE increase dramatically, often by a factor of 4 or more to ~150 ppm/^{o}C. Designing optical devices, especially single mode devices, to function with this amount of motion is very challenging. Hence, critical joints, meaning those that must not allow significant motion during the manufacturing and use cycle, usually exclude epoxies.

Uses:

Some common uses of epoxies are die attach to hold die in place, wire bond encapsulation to provide protection, underfill to strengthen flip chip and BGA joints, overmolding to provide environmental protection, other, specialized uses.

Modulus of Elasticity:
Epoxies with a wide range of room temperature modulus are available; from < 2Gpa (~300Kpsi) to > 20 Gpa (3,000 K psi). Above the Tg, the modulus can drop by a factor of 10.

Packaging:
Epoxies are inherently 2 part systems, traditionally a catalyst and resin. Electronic epoxies come in 2 forms:

- 2 part system. These are available and used but require mixing just before use and potentially de-gassing.
- Pre-mixed materials that are shipped and stored cold (typically <-40^{o}C). They are thawed, and at least kept dry if not actually dried, just before use. Drying is needed due to the potential for water condensation if the material is not stored in a dry environment or sealed contained.

Forms:

In addition to the 2 part systems that must be mixed and the premixed materials shipped and stored cold at -40C, epoxies are now being shipped as films. These films are very attractive in electronics for reasons explained below and of value in optical products.

Epoxy pastes and liquids:
After the epoxies are mixed or thawed, they are deposited on substrates using needle dispensing, auger dispensing that gives better quantity control, or stamping (like a classic hand stamp that might say "sold") to give specific shapes and a controlled quantity. The viscosity is important to controlling flow. Some epoxies have a high viscosity and stay exactly where they are placed, others, used for underfill or encapsulation have low viscosity and whose flow is thus influenced by capillary action or gravity.

Epoxy films:
The films are typically placed on the back of wafers before dicing as a b-stage. After dicing, the part, typically die, are placed on a heated substrate where the epoxy undergoes further curing holding the parts in place. The uniformity of the thickness, distribution and shape control result in highly predictable final part location.

Pot life:
Epoxies have varied pot life. Long pot life is good for manufacturing environments where material can be used over an extended period without the properties, especially viscosity, changing significantly and effecting the dispense pattern and subsequent flow. Some heavily loaded epoxies, such as those that have high thermal or electrical conductivity, contain a high percentage of volatiles that evaporate resulting in a short pot life.

Epoxy conductivity:
The three basic types are:

- Electrically conductive
- Thermally conductive (< 40 watts/m-^{o}C)
- Non conductive

Solder joints

Solder is used primarily to make electrical joints and is not very suitable for mechanical joints. Nonetheless, solder is sometimes used for that purpose, especially in conventional surface mount assembly technology where he mechanical stresses are minimal.

Solder alloys and their properties:
Many solder alloys with varied properties are in use. The classic solder is Sn63 meaning 63% tin and 37% lead by weight. That material has excellent properties for electrical joints but has fallen out of favor in recent years because of its lead content. (Lead can cause problems in biologic systems and is being eliminated from use in a variety of applications including electronic soldering under the RoHS regulations passed in many countries.) A common Sn63 replacement is the SAC alloys, alloys of tin (Sn), silver (Ag) and Copper (Cu). The designation SAC 305, for example, means an alloy of 3% silver, 0.5 % copper and the balance tin. Variations on this combination are common as is the use of other alloys containing Bismuth, Indium, etc.

In addition to eliminating lead, alloys are chosen for their cost, melting point, wetting characteristics, mechanical and electrical properties, sensitivity to tin whisker growth and other properties.

Classic Sn63 solder has the interesting property that it cold flows. If Sn63 is under mechanical stress, it will slowly slow to relax the stress. (A piece of solder wire with a weight hung from it will slowly stretch.) This property is good in electrical joints because the joints self-relax rather than break under stress. The latter is bad, of course, because breaking implies a complete separation of 2 parts that were joined resulting in an electrical open circuit. This cold flow property means that Sn63 is not good for mechanical joints that bear stress. Thus, classic electrical joints always had a mechanical connections means that was supplemented by solder to form a metal to metal continuously conducive electrical joint.

The cold flow property of Sn63 implies that that alloy is not particularly good for optical devices when mechanical stability is important. If any stress is placed on the joint, parts will move to relieve the stress potentially interfering with the optical functions.

The SAC alloys, however, do not cold flow and tend to be more brittle.

SOLDER FLUXES:

Solders must "wet" the surface of conductors to make a good intermetallic joint. Wetting is enhanced by cleaning conductive surfaces and removing oxides. The most common method of dong so us by using a "flux". Flu removes oxides and other surface contaminants so the liquid solder can come in direct contact and thus wet metal surfaces. In addition to being clean, the metal surface temperature must be above the melting point of the solder so the solder will stay in the liquid state.

Flux can be applied to the interfaces to be soldered in multiple ways. The most common is to mix a mild acid with an organic carrier and solder in the form of small balls to form what is called "solder paste". This material can be deposited with stencil printing, screen printing, needle dispensing, etc.; basically any method that puts the material where it is needed to form a joint. The most common method in electronic assembly is stencil printing that is usually done by automatic machinery.

In addition to applying flux in a paste, flux can be applied as a separate liquid which is sometimes done by putting the flux in the center of a wire made of solder. Hand soldering often utilizes that method of a flux applications. Wave soldering, and fountain soldering are processes that make a "hump" or "high spot" of melted hot liquid solder by pumping the solder. Flux is often applied as a foam or liquid. The advantage of the "solder hump" is a board, for example, can be moved over the "hump" without touching anything but the liquid solder.

A final method of applying "flux" is with a gas such as forming gas, 4% hydrogen, 96% nitrogen, with formic acid. These agents are strongly reducing and convert metal oxides back to base metal to enhance their wettability

In the case of the liquid or paste fluxes, they tend to leave a residue that can be detrimental both cosmetically and functionally. Thus, methods of removing this residue are inherent in soldering processes. The most common flux removal process is washing with de-ionized water. The flux system, of course, must be compatible with that process. Sometimes, soponifiers (soap) is often mixed into water to enhance the cleaning power of the water.

In electronic assembly, solder pastes referred to as "no-clean" are often used to eliminate the final washing step and issues associated with it. These solders leave behind a residue that is cosmetically detrimental, can effect high frequency dissipation factor and potentially contaminate optical surfaces. Thus, the no-cleans are not recommended for optical products unless they are cleaned, an increasingly common practice!

SOLDER JOIN LOCATION ACCURACY

The following issues must be addressed to maintain accurate part location in soldered joints.

When solder melts and reflows, parts can "float" and thus move, under capillary action to an equilibrium location established by the solder thickness and the extent and degree of wetting of both the substrate and the part. (Also, without some sort of solder stop, such as solder mask, solder can "wick" along a metal trace causing a part to move with it.)

When parts go through a reflow oven as they do in the standard surface mount process, the paste decomposes cleaning the surfaces, the solder melts so the parts being soldered are no longer held in place by the sticky solder paste. Thus not only capillary action and "floating" can move parts but so can air flow or the mechanical motion of a moving belt that "jiggles" parts while the solder is wet causing them to move. Thus, accurately placing parts during the conventional surface mount process is only part of the process of fixing parts with high accuracy in desired locations. The steps, after placement of transporting and reflowing the solder, need to be carefully considered o give high accuracy, repeatable results.

Finally, as solder solidifies, it shrinks a small amount thus causing further movement that may need to be considered for high accuracy optical devices.

MANUFACTURING EQUIPMENT

The joining methods reviewed above require equipment to implement the processes.

Electronic manufacturing equipment is generally the starting point when seeking assembly methods for optical devices. That said, electronic assembly equipment tends to lack several characteristics important for optical assembly;

1. Tolerance control
2. Emphasizes planar assembly vs assembly in the Z dimension that optics sometimes requires.

Those limits aside, electronic equipment is attractive due to the low costs attainable when it is suitable. Electronic assembly equipment is built in relatively high volume, is widely available and typically has high assembly rates (10,000+/- parts/hr.). Thus many optical assembly processes utilize conventional electronic assembly equipment and processes that may be modified to enhance its suitability for optical device assembly.

Manufacturers now make equipment that is able to place parts with an accuracy of 0.5 microns. The table below summarizes the capabilities and the figures following illustrate some of the equipment available. The price of this equipment ranges from <$100K to >$750K depending on the supplier, the capability, the assembly rate and the options selected. Most equipment is custom built to the buyer specifications for high volume applications.

The table is a simple summary of the 5 examples of currently available high accuracy placement equipment that follows. Typically the equipment manufacturers measure the throughput as the time for a die bonding machine to pick-and-place a die onto a carrier with the target accuracy. Additional process time, required to complete the joint formation between the die and the carrier, is mainly dictated by the product and process design and will add to the overall cycle time. In order to achieve certain levels of high accuracy, e.g., 0.5μm or better, a special near field optical alignment unit is typically deployed between the pick-and-place period, which should be included in the pick-and-place throughput figure. The near field optical alignment needs alignment fiducials on the die and the carrier, and sometimes on pick-and-place tools. Those fiducials need to be high quality optically and high precision dimensionally in order to achieve high accuracy - similar to the requirement in semiconductor wafer level lithography processing.

Supplier, Model	Placement Accuracy, microns	Place Rate, UPH	Flexibility	Cost
Semiconductor Equipment Corp, SEC 850	+/- 1.0	~60		
Fine Tech, FINEPLACER sigma	+/- 0.5	240		
MRSI, MRSI-M1	+/- 0.5	450		
Palomar, 6500 Die Bonder	+/- 1.5	1200		
K & S, APAMA	+/- 1.0	<3000		

The last item, the K & S APAMA, differs from the other 4 in that it is specifically designed and used for a process called Thermocompression bonding in which solder capped copper pillars with a pitch < 60 microns are bonded utilizing an in-situ heating and cooling process to make joints utilizing solder and sometimes underfills. This process is intended for use with high density, high IO (>1000) contact devices such as microprocessors, ASICS and some memory devices. The force available to "squash pillars and solder caps to bring these point to be joined into contact over the typically relatively large area (25 mm x 25 mm) is up to 300 Newtons (~ 66 #s). While most optical devices do not have these high IO counts, some proposed devices such as optical interposers may in the near future.

SEC 860 Specifications

- High accuracy, within 1-2 microns
- Custom systems for your specific application
- Fast and easy set-up
- Compact footprint
- Intuitive Windows based operating system
- Low maintenance with minimal calibrations
- Select only the options you need

Fine Tech

FINEPLACER Sigma

Fine Tech FINEPLACER Sigma Specifications

- 0.5 micron accuracy
- 15 sec/placement + process time
- Up 300 mm substrates
- Up to 500 Newtons force
- Attachment Methods
  - Die Attach Film
  - Gold-Tin Eutectic
  - Gold thermocompression bonding
  - Thermosonic bonding
  - Solder Reflow
  - UV cured polymers

MRSI Systems, MRSI-M-1

MRSI-M1 by MRSI Systems (www.mrsisystems.com)		
Placement cycle rate (process time additional)* * Application Dependent		450 UPH at 3 μm (M3)
Smallest die		250 μm
Placement accuracy (3 sigma)		3 μm true radial position (M3)
		1 μm with camera probe (M1)
Repeatability		<1 μm
Z axis place to force or height (standard)		Programmable force 10g to 5Kg Optional force 500g to 50Kg
X travel		443 mm (17.5”)
Y travel		911 mm (36”)
Z travel		38 mm (1.5”)
Theta travel		360°
Angular resolution		0.00045°
Available configurations	Die Attachment. Flip-chip Bonding and Thermal Compression Bonding optional.	
	Eutectic and Epoxy process or integrated dual process. UV Attach optional.	
	Dies can be picked from Gel-Pak, waffle pack, wafer, and tape & reel.	
	Automatic system conveyor handles boards, fixture trays, boats, and lead frames.	
	Automatic wafer loading and unloading from cassette for multiple wafer handling. Wafer processing includes wafer mapping and ink dot detection.	

Palomar 6500 Die Bonder

Palomar 6500 Die Bonder Specifications

CYCLE TIME
Up to 1200 UPH

POST-PROCESS ACCURACIES
1.5 micron (post-eutectic bond)

PLACEMENT ACCURACY
3 micron, 3-sigma ultra-high accuracy eutectic and adhesive placements with cycle time of approximately 3 seconds

MULTIPLE OPTIONS
Pulsed heat stage/steady state for eutectic attach, flip chip, tape feeders, magazine handlers, ID tracking software, look-up camera software, in-line assembly lines, islands of automation, fully automatic substrate and part loading

LARGE WORK AREA
12.5 inch x 6 inch (317.5mm x 127mm) X/Y six position, bi-directional turret tool changes tools rapidly.
High-speed, four-axis positioning system

Process Requirements	Specification 2015
Thin die handling (TSV 10:1) Die thickness	≥ 35 um
Fine pitch Cu Pillars Accuracy	± 2.0µ, ±20 mdeg, post bond (3σ) ±1.0µ, ±10 mdeg, glass die (3σ)
Cu Pillar Stacking Planarity	2µ / 10mm
High force capability	0.5 to 300N
Process Control Force Accuracy	0.25N or 1% (whichever larger)
Bond Line Thickness Z-Height Resolution	± 1.0µ (with temperature compensation)
Low COO – Productivity	Heat Ramp: > 200C/s
	Cool Rate: >100C/s
	Dry Cycle: <1.5 sec
	Sprint UPH: 3000 DH
Yield and Metrology	Die crack detection Contamination inspection Post bond overlay IR Align NCF

QUALITY/RELIABILITY

The quality and reliability requirements for optical devices are comparable to those for other products, especially electronic devices. Optical data communication products typically have a lifetime of 10 years or less. While some optical data communication products are still built to the Telcordia 40 year standard, most products, even those used in communication do not need to be qualified to that standard.

These optical products, materials and processes, especially those utilizing new materials, processes, components and technology, do need to undergo rigorous qualification testing. Ideally each of the new processes and materials will be carefully evaluated and qualified to ensure they will perform over an extended lifetime in the environment and under the conditions they may encounter.

ENVIRONMENTAL ISSUES AND TECHNOLOGY

Concerns have been raised concerning the use of some elements in optical devices. Lead in conventional solder must be excluded and lead free alloys utilized. Concerns have been raised about arsenic and nickel with some efforts underway to exclude these elements from commercial products. Cadmium, lead and mercury, of course are currently banned from new products under the RoHS requirements.

Most optical devices do not utilize undesirable organics that are the subject of much of the current and emerging REACH requirements. These compounds are most likely to be found in optical devices used to do analysis where the compound interacts with some aspect/material/organism in the environment and generates a signal that optical technology is able to detect. (We may be faced with the dilemma of utilizing detrimental compounds to detect other undesirable compounds.)

The WEEE requirements related to recycling and disassembly have impacted optical products in only a minimal way to date. As optical devices proliferate, especially if they incorporate materials or elements that are viewed as detrimental, they will be scrutinized. Excluding these materials in new designs may forestall regulator issues.in the future.

Finally, the Conflict Materials Requirements of the US SEC require publically traded US companies to report the consumption of conflict materials, materials like gold, tin and tantalum, which come from certain parts of Africa. Thus, customers are asking suppliers to verify that the materials used in the products they buy do not contain materials from these sources.

TEST, INSPECTION, MEASUREMENT (TIM)

The most demanding test requirements are found in single mode applications so those are addressed below. Multimode signal testing is usually less demanding.

The Telecom Industry utilizes single mode technology over hundreds of kilometers and has led the development of optical test equipment and capability. Much of that equipment can be adopted for use with products being developed for the emerging needs for shorter distances.

Data communications test needs differ from Telecom in that they tend to utilize more parallel signal transmission through parallel media, either ribbon fiber or waveguide arrays, transmit light shorter distances and hence are not impacted as much by dispersion impediments and sometimes utilize more complex modulation schemes.

The general optical signal technical properties and test parameters follow in the table below.

Optical Test Parameters, Values, Media and Ranges		
Parameter	**Range**	**Comment**
Optical Signal Characteristics		
Wavelength	650 nm to 1,700 nm	These are the primary wavelengths used for optical communications. Longer, and sometimes shorter, wavelengths are used in sensors and analytic applications.
Optical power	<1 watt (30 dBm). usually < 0.1 watt(20 dBm)	This value applies to most communications, sensor and analytic applications. Much higher power levels are used for industrial processes. Laser safety must be considered.
Wavelength spacing	Down to 25 GHz or ~0.2 nm at 1.5 microns	Applies in dense wavelength division communications multiplexing (DWDM) applications. More demanding in some sensors.
Optical Modulation Rate	<28 GHz near term, 100 GHz long term	This is the typical On-Off keying (OOK) single frequency, single polarization, single phase amplitude modulation rate.
Laser Sources	40 Gbs/channel and higher	Reliable laser sources for 40 Gbs/channel and higher rates utilizing higher order modulation are needed.
Optical Amplitude Modulation	Up to 32 levels (5 bit) per single phase near term, 1024 levels (10 bit) long term	Long term both the I phase and the orthogonal Q phase can be modulated with up to 1024 levels implying a spectral efficiency of 20 bits per hertz or 200 THz X 20 = 4000 Tb/second on a single wavelength

Polarizations	2	Usually X and Y for SM. More complex for MM. Much more complex schemes are being explored.
Detectors	Responsivity	~1Amp/Optical watt (i.e. 1 milliamp with 1 milliwatt, 0 dbm of optical power.
Detector bandwidth	<28GHz near term, 100 Ghz long term	Going beyond ~50 GHz requires detectors ~ 1 micron in diameter resulting in complex challenges and maybe implementing plasmonic detectors.
Probing		
# of simultaneous optical drive test signals needed	1 to 4 near term, up to 1024 long term	Some number of optical test signals may need to be injected simultaneously into ribbon fiber or parallel optical waveguides with a combination of the following characteristics; one or more wavelengths modulated with controlled polarization, phase and/or amplitude with known and controlled skew between fibers.
Physical connections; Input of test signals and output of device signals	1. Conventional optical fiber connectors 2. Specialized for-test-only gratings built into substrates and products 3. Focused beams 4. Spliced fibers	A variety of probes (methods to get light into and out of optical ports, such as fibers, waveguides or elements such as lenses, mirrors, etc.) are likely to be required. For SM applications, alignment of the probes to the DUT (device under test) of < 0.5 microns, sometimes <0.1 microns will be required. MM applications require <5 micron alignment. Cleaning and inspection are required for each connector end contact face before mating with another connector to perform a test.
Test Detectors	Typically -30 dbm or higher, 650 nm to 1,700 nm, up to 50 Ghz	Need to measure power level, wavelength, polarization, latency and eye diagrams with up to 1024 signal levels (32 x 32 constellation). Also phase and skew between parallel signals.
Bit Error Rate (BER)	$< 10^{-9}$ to $< 10^{-12}$	BER is highly dependent on signal-to-noise ratio, signal conditioning, the application and the degree of error correction coding used, if any.
Optical Communication Signal Media Properties		
Single Mode Fiber	Typically 6 micron diameter high index (~ 1.5) glass core, 125 micron diameter lower index (~1.45) outer glass cladding, overall diameter of 250 microns with 125 micron polymer buffer.	
MultiMode Fiber	50 to 60 micron diameter high index (~ 1.5) glass core, 125 micron diameter lower index (~1.45) outer glass cladding, overall diameter of 250 microns with 125 micron polymer buffer.	
MultiCore Fiber	Recently developed for SM applications. Initially 7 SM cores in a 125 micron diameter with other combinations under consideration.	
Ribbon Fiber	Either SM or MM fibers built as a linear array, usually on 250 micron centers.	
Waveguides	Single mode from 0.5 microns to 6 microns, typically with a rectangular, near square cross section. Multimode larger, maybe to 100 microns. Both SM and MM waveguides are built in silicon, glass and polymers. Waveguides are typically no more than a few cm long as they tend to have higher attenuation that fiber.	

The following series of tables address Key Topics including needs, gaps, show stoppers

Roadmap of Quantified Key Attribute Needs						
Parameter	**2015**	**2017**	**2019**	**2021**	**2023**	**2025**
SM fiber attach to substrate, sec/joint	300*	240	192	154	123	98
SM part placement to <0.5 micron accuracy, sec/part	20*	16	13	10	8	6
MM part placement to <5.0 micron accuracy, sec/part	5*	4	3.2	2.6	2.0	1.6
	*decreasing 80% every 2 yrs.					

Degree of Integration	The greater the amount of parallel processing usable in fabrication, the lower the cost.
Number of parts	Minimizing the number of parts that need to be purchase, shipped in, inspected, inventoried, issued to manufacturing, assembled, tested and inspected reduces the cost of products.
Cycle Time for an Assembly	The second most important cost driver is the amount of time needed to build a device. This is the time which equipment or individuals apply to each device; waiting time in ques is excluded. Each step is typically assigned a $/minute that is charged to a device along with the part costs and overhead rates (usually a % of the prior costs) to establish the total cost.
Joining time	A key contributor to the assembly time is the time to form joints. Solders, for example, must cool, epoxies cure to at least a B- stage, welds must cool, etc. Minimizing these times minimizes cost.
Optical chain movement over time	Many single mode devices, that are expected to dominate optical devices in the long run, require stability of location over the lifetime of the product of 0.1 microns.
Part presentation	Minimizing assembly time requires minimizing the time needed to handle and feed parts to the assembly processes, especially machinery. Shipping parts as sawn wafers on tape or die attach film, in tape & reel, in trays, in waffle pack, or other standard method minimizes handling, losses and damage, all of which reduce cost.
Test time	Testing is often expensive, especially design verification and the engineering of software and fixtures for in process and final testing. Long test cycles can raise cost rapidly if expensive test sets are needed.

Key Attribute Needs #1

Parameter	Metric	2013	2015	2017	2019	2025
Assembly	#REF!					
Single Mode Fiber attach to substrate	sec/joint	300	240	192	154	98
Single Mode Part Placement to <0.5 microns accuracy	sec/joint	20				
Multi-mode Fiber attach to substrate	sec/joint	300	240	192	154	98
Multi-mode Part Placement to <5.0 microns accuracy	sec/joint	5				
Package Costs	#REF!					
IC Package Cost	¢ per I/O	0.18	0.16	0.15	0.15	0.12
Package Cost (High Density Ceramic/w/ Area Connector)	¢ per I/O	5	4	3	2	1
Package Cost (High Density µvia Laminate w/ Area Connector)	¢ per I/O	4	3	2	2	1
Connector Cost	¢ per I/O	1.90	1.6	1.3	1	0.5
Energy Cost	$/Wh	0.40	0.30	0.25	0.20	0.10
Memory Cost (Flash)	$/MB	0.18	0.15	0.13	0.10	0.05
Memory Cost (SRAM)	$/MB	0.18	0.15	0.13	0.10	0.05
Cost of Test as a ratio to assembly	ratio	0.40	0.50	0.60	0.60	0.80
Cycle Time						
NPI Cycle Time	Weeks	20	16	12	6	3
Product Production Life (not including spares)	Years	7	6	5	3	3

Key Attribute Needs #2

Parameter	Metric	2013	2015	2017	2019	2025
Reliability						
Temperature Range	Deg C - Deg C	-40 to 85	-40 to 85	-40 to 85	-40 to 85	-40 to 85
Number of Cycles	Cycles to Pass	1000	1000	1000	1000	1000
Vibrational Environment (PWB level)	G^2/Hz	0.03	0.03	0.03	0.03	0.03
Use Shock Environment	Gs & ms to Pass	50G (2ms)	50G (2ms)	50G (2ms)	50G (2ms)	50G (2ms)
Stability of Optical Alignment						
Devices	#REF!					
Number of stacked die (Max)	#	3	4	6	6	9
Number of Die in SiP (max)	#	6	7	7	9	12
Electrical & Test						
Frequency on Board	MHz	10K	25K	40K	100K	1000K
Impedance Tolerance	%	7	7	5	5	3
Number of Voltages	#	10	10	12	12	14
Off Chip Driver Rise Time	V/ns	25	30	35	50	100
Serial Bus Rate (1 bit)	Gb/s	8	10	14	24	40
Built In Self Test (BIST)	%	50	70	85	90	95
Boundry Scan	%	20	35	50	75	85
Test pad access minimum	%	25	20	15	5	3
Maximum escape rates	DPMO	500	400	300	200	100

TECHNOLOGY NEEDS:

Prioritized Development & Implementation Needs (< 5 years result)
Minimize the number of parts and number of assembly steps
Metal to metal, epoxy, or alternate joining methods that are fast and provide stable joints over the life of the product.
Developing the properties of standard materials for use in design.
Design software able to utilize Hooke's General Law over temperature to ensure designs will function over the life of the product.
Self-alignment/passive alignment (must avoid active alignment and testing to go to high volume)
Standardize transmission media for short distances • On chip waveguides • On circuit board waveguides • Connectors for and to the above • Mode converters to SM fiber • Test interfaces
Standardize platforms and parts • Receiver • Transmitter • Transceiver • Multiple optical IO need to be standardized for each family
Improved machine intrfaces to minimize programming and set-up time to reduce costs for short optical product runs.
Develop a budgeting method for product development • More training of designers in Design for Manufacturing, Test and Cost

Prioritized Research Needs (> 5 years result)
Process to build reliable light sources that can be modulated at 50Ghz+ compatible with CMOS
Highly integrated devices to minimize part count and the need for assembly
Assembly equipment customized specifically for specific optical requirements
Ability to locate parts to sub-micron tolerances.
Software methods to simulate manufacturing processes to enable more rational selection of materials, processes and equipment
Methods to fabricate optical components with sub-micron tolerances at low cost.
High tolerance substrates/platforms that optical components are assembled on, possibly made with 3d printing and laser finishing.
Nano-materials with improved properties
Meta materials to provide new functionality
Integrate packaging into the device rather than putting an optical structure into a separate package

Erasable grating to put optical probe points on a chip without impacting the performance after the chip is packaged.
Structures to convert light to plasmons to reduce the size of high frequency detectors

GAPS AND SHOWSTOPPERS

Gaps and Showstoppers
Continual improvement in electrical transmission methods keeping electrical methods less expensive than optical solutions
High cost resulting from the difficulties of integrate/combining a suitable light source with CMOS electronics
Difficulty eliminating Active Alignment
High costs resulting from low production volume due to limited applications and lack of standard methods
Component attach processes, and joining methods generally, that cause micro motion such as creep with epoxy during the curing step
Speed of suitable assembly, test and other process equipment resulting in high costs.
Joining processes with long cure/joining/cooling cycles that raise cost
Inability to overcome the cost driving, rate limiting step/bottle neck of manufacturing/testing Such as the Duration of UV or thermal cure steps and the number of assembly steps ? **"Time is money"**
Limits resulting from adopting existing equipment, materials and methods to optical assembly and test
Difficulties building in the Z dimension often required by optical devices
Achieving low cost heterogeneous assembly of III-V parts with CMOS devices.
Fabricating optical transitions from one media or device to another that minimize loss and alignment cost
Limited availability of manufacturing simulation tools and software
Designing for Manufacturing and test: • Maximizing output to reduce cost • Studying designs to trade off accuracy and speed
Inability to utilize materials or processes due to environmental related constraints (RoHS, REACH, WEEE, etc. TBD)

RECOMMENDATIONS ON POTENTIAL ALTERNATIVE TECHNOLOGIES

Recommendations on Potential Alternative Technologies
Explore the use of 3D printing to build a suitable substrate/platform upon which optical components can be placed, affixed and assembled in 6 dimensions that have smooth surfaces meaning to <0.1 microns RMS roughness.
Review the history of platforms for passive assembly (silicon optical bench) that have well defined mechanical stops and associated methods to affix/weld/glue parts in place and classify their characteristics for highly accurate optical assembly.
Explore methods utilizing capillary actions to “Pull” parts into place to effect passive alignment.
Utilize laser machining to do micro and nano cutting and shaping to make highly accurate parts to implement passive optical alignment.
Utilize laser processing to make optical waveguides in-situ to effective optical connections and optical structures.
Utilization of plasmons to minimize size and maximize functionality

Silicon Photonics System Assembly Roadmap 2015-25

Parameter	2015	2018	2025	2035	Emerging Assy Technology	Difficult Challenges/ Roadblocks
Chip Attach	CSP C4, uBGA	3D Die Stack PoP	PoP, SoC	PoP, SoC	Heterogeneous Wafer-Scale Pkg.	
Chip Pkg.	BT-SMT	BT-SMT	Si-SMT	Si Integrated	Panel Process - WG	
Multi-Chip Pkg.	HDI-SMT	HDI-SMT-PoP	HDI-SMT-PoP	Si Integrated	Panel Process - WG	
Module Pkg.	Hetero.	Hetero.	Panel Process	Si Integrated	Panel Process - WG	
Main Board Pkg.	Conventional FR4, Fly-Over Fiber	Same	Fly-Over + Embedded WGs	Embedded WGs	System Shrink to SiPh Module, Poss. Printed/Embossed	
Transceiver Pkg.	InP Die-Module	Si Die PoP Module	SiPh DoD	SoC	Wafer Scale SiPh (AIM Award)	
R-C Passive Chips	Bench	Shooter	Embedded	Embedded	Printed Electronics	
Discrete Fibers, Waveguides	MM Fibers	SM Fibers PWGs	SM Fibers Free-Space PWGs	SM Fibers Free-Space PWGs	All-Optical ICs w/ SM Glass WGs	

Process	Status of Assembly Process	2018 Key Parameter	2025 Key Parameter	2035 Key Parameter	Emerging Assembly Technology	Difficult Challenges/ Roadblocks
Wire Bonding	Mature					
C4 Die Attach	Mature					
Wafer-Scale Pkg.	Emerging					
DoD	Production					
POP	Production					
Micro-SMT	Production					
SMT	Mature					
Chip Shooters	Mature					
Pick & Place Equip	Mature					
IC Packaging	Mature					
Multi-Chip Pkg.	Production					
Transceiver Pkg.	Production					
Module Pkg.	Production					
Organic PCB Pkg.	Mature					

Comments: Key to the future of SiPh manufacturing is the supply of SiPh chips. There may be a tendency for key suppliers to retain control of IP, with a small group of 'approved' collaborators. This could delay widespread use of SiPh systems and slow assembly technology development. As a domestic US venture, most of the equipment and processes went global. IC packaging and organic substrates are centered in Asia. Key assembly equipment suppliers are Japanese. It is in semiconductor manufacturing where a major US presence exists. Existing transceiver manufacturing is InP discrete modules, which must transition to a heterogeneous and eventual monolithic Si designs. Availability of assembly processes for early and later SiPh systems will endure a chicken-to-egg timing issue.

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APPENDIX B[5] - GENERALIZED HOOKE'S LAW

Axial Strain:

$$\varepsilon_x = \frac{1}{E}\left[\sigma_x - \nu(\sigma_y + \sigma_z)\right] + \alpha\Delta T$$

$$\varepsilon_y = \frac{1}{E}\left[\sigma_y - \nu(\sigma_x + \sigma_z)\right] + \alpha\Delta T$$

$$\varepsilon_z = \frac{1}{E}\left[\sigma_z - \nu(\sigma_x + \sigma_y)\right] + \alpha\Delta T$$

Shear Strain:

$$\gamma_{xy} = \frac{\tau_{xy}}{G}$$

$$\gamma_{yz} = \frac{\tau_{yz}}{G}$$

$$\gamma_{zx} = \frac{\tau_{zx}}{G}$$

$$G = \frac{E}{2(1-\nu)}$$

Where:

ε = Strain
γ = Shear Strain
σ = Stress
τ = Shear Stress
E = Young's Modulus
G = Shear Modulus
ν = Poisson's Ratio
α = Coefficient of Thermal Expansion
T = Temperature
Stress and strain can have negative and/or positive values to represent tension and/or compression.

APPENDIX C - ACRONYMS, DEFINITIONS AND GLOSSARY

This table contains terms used in optical technology. Not all are used in this chapter.

Common Optical Electronics Abbreviations and Terms	
2.5 D and 3.0 D	2.5 D Often refers to an electronic packaging method in which semiconductor die are interconnected through a larger part, often called an interposer or substrate, often fabricated on silicon with vias, electrical interconnections and electrical contacts such as solder balls. 3.0 D Refers to stacking multiple semiconductor die on one another and interconnecting them utilizing wire bonding or TSVs.
3D	3 Dimensional printing. A process coming into wide use to fabricate parts by "printing" them, usually by depositing the base material in small particles, from a liquid or some controlled micro-stream.
3R	Reamplification, Reshaping, Retiming
AOC	Active Optical Cable. By definition, has no optical connector.
APD	Avalanche Photo Diode

[5] "Engineering Mechanics of Solids Egor P. Popov

ASICS	Application Specific Integrated Circuits
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
BGA	Ball Grid Array. Usually used in reference to the IO pattern on an integrated circuit package. Balls are typically arranged in square arrays.
CAT 5	A type of copper cable with twisted pairs to operate at 100 Mbs and higher data rates.
CATV	Cable Television
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing. A method used to planarize devices, typically used to fabricate the interconnect layers on an integrated circuit. Similar to lapping.
CNT	Carbon Nano Tube
CTE	Coefficient of Thermal Expansion
CPU	Central Processor Unit. Also a Microprocessor.
CWDM	Coarse Wavelength Division Multiplexing
CXP	A high density transceiver form factor
DAF	Die Attach Film. Typically applied to the back of a semiconductor wafer before dicing so that the die has adhesive on it and is ready for placement on a substrate or package.
DBI	Direct Bond Interconnect. A method of joining surfaces by making them extremely flat with surfaces that will molecularly bond such as SiO_2.
DBR	Distributed Bragg Reflector
DCF	Dispersion Compensation Factor
DFB	Distributed Feedback
DPSK	Differential Phase Shift Keying
DSP	Digital Signal Processor
DWDM	Dense Wavelength Division Multiplexing
EDFA	Erbium-Doped Fiber Amplifier
EMI	Electro Magnetic Interference
EML	Externally Modulated Laser
ESD	Electrostatic Discharge
FC	Fiber channel. A standard protocol for Mass Storage

FDDI	Fiber Digital Data Interface
FEC	Forward Error Correction
FR-4	Fire Retarded- version 4. The most common epoxy glass circuit board dielectric material.
FR-5	Fire Retarded- version -5. Similar to FR-4 but with higher temperature tolerance.
FTTx	Fiber to the X (Home, Office, Curb, Node, etc.)
Gb/s & Gbs	Gigabits per Second
GH or GHz	Gigacycles per second.
GI	Graded Index, a type of optical fiber
HDMI	High Definition Media Interface
HVAC	Heating, Ventilating and Air Conditioning
HFC	High Frequency Component
Hz	Cycles per second
I	One of two phase in QAM modulation. Q is the other. I and Q are at 90^{o} to each other.
IO	Input Output. Usually used to refer to the inputs and outputs of a device, either electrical, optical or other.
III-V	Periodic Table, Group III-V Elements. Refers to semiconductor materials such as GaAs, InP, etc.
II-VI	Periodic Table, Group II-VI Elements
IC	Integrated Circuit
IO	Input Output
IP	Intellectual Property
IQE	Internal Quantum Efficiency
ITRS	International Roadmap for Semiconductors
ITU	International Telecommunications Union
JISSO	Japanese Term Reflecting The Total Packaging Solution For Electronic Products
LAN	Local Area Network
LCD	Liquid Crystal Display or Liquid Crystal Device such as a modulator
LED	Light Emitting Diode
MOST	Media Oriented Systems Transport. A 100mb/s in-vehicle automotive multimode optical standard usually implemented with POF.

MM	Multimode.
MSA	Multi-Source Agreement
MZ	Mach-Zendher. A type of intensity modulator for single mode light
OADM	Optical Add Drop Multiplexers
OC-48	Optical Carrier 48 (see SONET specification GR-253-CORE). ~ 2.5 Gb/s data rate.
ODM	Original Design Manufacturer
OE	Optoelectronic
OECB	Optoelectronic Circuit Boards
OEM	Original Equipment Manufacturer
O-E-O	Optical to Electrical to Optical
OIDA	Optical Industry Development Association
ONU	Optical Network Unit
O-O	Optical to Optical
OOK	On Off Keying. A modulation method in which the carrier is turned on and off to imprint information on the carrier.
OSA	Optical Sub Assembly
pJ	Pico Joule. 10^{-12} Joules.
PCB	Printed Circuit Board
PCS	Polymer Clad Silica
PD	Photo-Diode
PEG	Product Emulator Group. 5 iNEMI groups defining technology needs by product class.
PIC	Photonic Integrated Circuit. Usually an active semiconductor chip.
PIN	Photodetector. A diode with an Intrinsic layer between an N layer and P layer.
PLC	Planar Lightwave Circuit. Usually a passive waveguide structure
PMMA	Polymethyl Methacrylate
POF	Plastic Optical Fiber
PON	Passive Optical Network
POP4	A transceiver form factor
PPOF	Perfluorinated Plastic Optical Fiber
PVC	PolyVinylChloride. A flexible polymer often used in cable jacketing
QAM	Quadrature Amplitude Modulation

QFSK	Quadrature Phase Shift Keying
QSFP	A transceiver form factor
REACH	An emerging standard to control hazardous materials
RF	Radio Frequency
RIE	Reactive Ion Etching. A process used to remove material to fabricate semiconductor and other devices with small features.
RMS	Root Mean Square. A standard method of conveying variation in a parameter such as surface roughness or sine wave voltage.
ROADM	Reconfigurable Optical Add Drop Multiplexer
RoHS	Restriction on use of certain Hazardous Substances
ROSA	Receive Optical Sub Assembly
Rx	Optical Receiver
SAC	Abbreviation for SnAgCu, a class of solder alloys that are lead free and require higher reflow temperatures than conventional lead tin SnPb, (Sn63) solder
SAN	Storage Area Network
SFF	Small Form Factor
SFP	Small Form factor Pluggable
SI	Step Index. Refers to the refractive index between fiber core and cladding.
SiP	System in Package
SM	Single Mode
SMF-28	Single Mode Fiber (standard version)
SMT	Surface Mount Technology
SNR	Signal to Noise Ratio
SNAP12	A transceiver form factor
SOA	Semiconductor Optical Amplifier
SoC	System on Chip
SONET	Synchronous Optical Network (see SONET specification GR-253-CORE)
SOP	System on Package
T&M	Test and Measurement
Tb/s & Tbs	Terabits per second
TEC	Thermo-Electric Cooler
THz	Terahertz.
TIA	Trans Impedance Amplifier

TOSA	Transmit Optical Sub Assembly
TSV	Through Silicon Vias
TWG	Technology Working Group.
TV	Television
Tx	Tx: Transmitter
ULSI	Ultra Large Scale Integration
UPH	Units Per Hour. Usually used to quantify manufacturing process rates.
USB	A type of computer port and connector
UV	Ultra Violet
VCSEL	Vertical Cavity Surface-Emitting Laser
VOA	Variable Optical Attenuator
VLSI	Very Large Scale Integration
WDM	Wavelength Division Multiplexing
XAUI	10 Gb/s Attachment Unit Interface (see IEEE 802.3ae)
XFP	10 Gb/s small Form factor Pluggable
xGE	X Gigabit Ethernet
XENPAK	A transceiver form factor
XPAK	A transceiver form factor

APPENDIX A: PSMC ROADMAPPING PROCESS

The PSMC roadmapping process is based on the iNEMI/ITRS process. This process is a bottoms-up Delphi process, relying on numerous technology experts to give their vision of the technology needs that must be developed to meet their view of the products of the future.

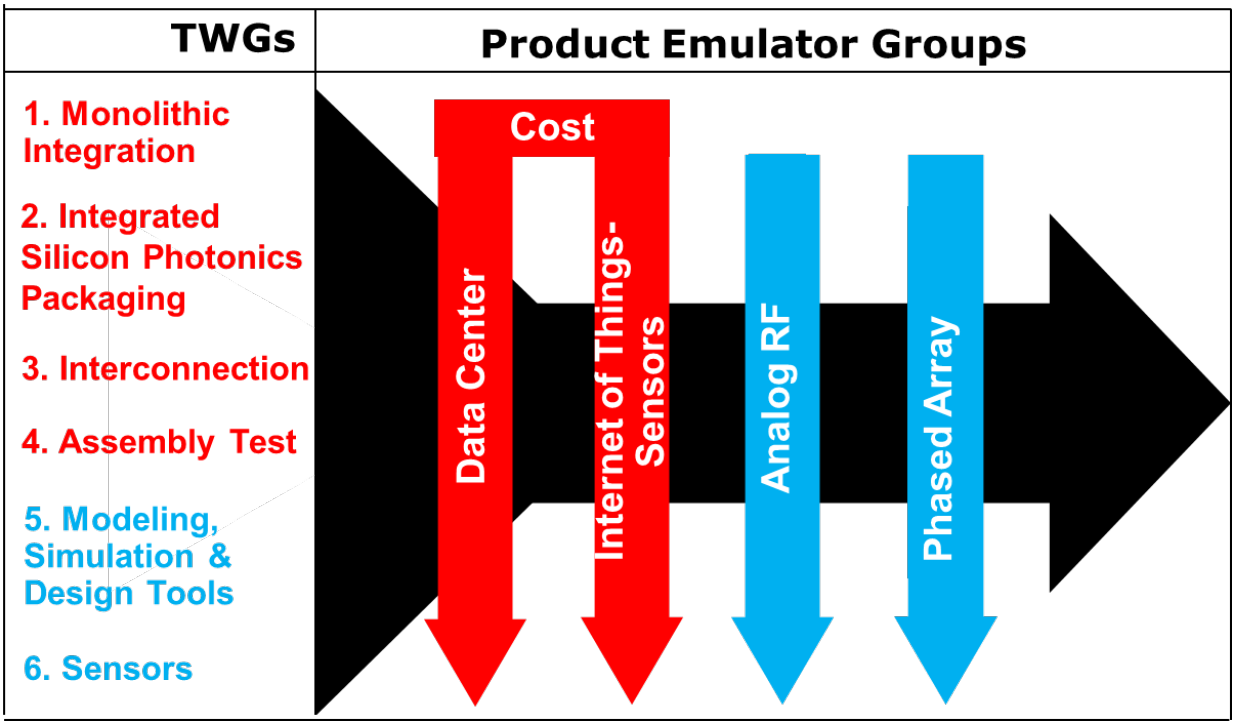
The Delphi technique[1], developed by Dalkey and Helmer at the Rand Corporation, is a widely used and accepted method for achieving convergence of opinion concerning real-world knowledge solicited from experts within certain topic areas. The roadmapping process does not explicitly identify disruptive technologies, but by identifying needs, particularly those for which there are no known solutions that meet the performance and cost requirements, members of the PSMC roadmapping team implicitly identify areas for innovation and the utilization of disruptive technologies.

The restructuring of the electronics industry from vertically integrated firms to specialized firms has stimulated discussion on how the industry can effectively develop and implement disruptive technologies such as integrated silicon photonics, to ensure the continued growth of the global electronics industry. As we continue to combine disparate technologies into product architectures, a number of integration challenges face the industry. What once was a multi-board system is now a chip. These rapid reductions in size and increases in speed require new approaches to performance. At the same time, the business model has changed, and the ability to do full systems engineering within a single organization such as IBM or AT&T is no longer possible. This change in structure has led to a number of areas where collaboration is required to achieve the necessary level of optimization. Suboptimal solutions can limit our ability to improve performance, cost, size, and reliability.

This roadmap is the product of numerous large and small meetings between industry, government, and academia that took place over a period of eighteen months. The roadmapping process engaged scientists, researchers, and executives from throughout the supply chain in the study and prioritization of the challenges facing the manufacture of low-cost high-volume integrated silicon photonics.

The 2015 Roadmap was developed by three Product Emulator Groups (PEGs) and four Technology Working Groups (TWGs). These groups included more than 400 participants from over 160 private corporations, consortia, government agencies, and universities in eleven countries. The following figure illustrates in red the seven groups that developed this roadmap. We are currently in the process of establishing the four groups shown in blue for our next roadmap. These additional groups will increase the completeness of our technical planning

[1] Dalkey, N. C., & Helmer, O. (1963). An experimental application of the Delphi method to the use of experts. *Management Science, 9* (3), 458-467.



The PSMC Roadmapping Organization consisting of the members of the PSMC Leadership Committee, Product Emulator Groups from three sectors of the photonics industry, and the members of four Technology Working Groups (TWGs) was assembled to identify the key technology and infrastructure needs of the global integrated silicon photonics manufacturing industry. The Roadmapping Organization was spearheaded by industry. The document is divided into four independent (but complimentary and consistent) technology roadmaps on topic areas deemed important by the PSMC Leadership Group. Each technical roadmap was prepared by a TWG and has associated with it one or more Gaps, Showstoppers, and Recommendations. In future roadmaps we anticipate expanding the number of TWGs. The PSMC is committed to improving the roadmapping process; to identifying disruptive technologies; to finding solutions to current needs; and to help anticipate new applications and products.

The structure of the roadmaps and the editing of this document were led by the Principal Investigators. An effort was made to keep the roadmapping process as open as possible and to include all constructive inputs as part of the final roadmap document. The process was opened to global participation and review, including Europe and Asia. Each technology roadmap, although written as a stand-alone section, inter-relates with other topics referenced in this document and may also refer to other industry roadmaps.

The Roadmaps were developed by the four Technology Working Groups, and two Product Emulator Groups of the Roadmap Organization consisting of more than 400 individuals recruited from more than 160 organizations. Each PEG (with TWG feedback) was asked to complete an "Excel" spreadsheet, consisting of a quantified roadmap of key attribute needs for each of the four specific years (2015, 2017, 2019, 2025). The TWG Chairs were also

challenged to forecast potentially disruptive technologies that might appear in the 2019 - 2025 time frame – in order to focus on the most strategic aspects of the roadmap.

Major PSMC roadmap meetings, each attended by approximately 100 participants were held in Cambridge Massachusetts in April 2014, November, 2014, and April 2015. One purpose of these workshops was to present the developing findings of the Roadmap Organization to a wider audience for input. Workshop participants from industry, academia, and government were given the opportunity to comment on the document and make recommendations on the findings. Maximum flexibility was given to the groups to identify and pursue any and all topics they felt were relevant to the PSMC goals. Each TWG chair gathered needs and priorities from a variety of experts. Each roadmap lists some of the experts who participated.

A technical review of each chapter draft was carried out by members of the PSMC Leadership Committee and/or the PSMC Executive Steering Committee. The final written document was edited by Robert C. Pfahl, PSMC Principal Investigator and Jim McElroy, PSMC Executive Director

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