Power-efficient Delta Readout Scheme utilizing Multi-Column-Parallel SAR ADCs

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Abstract This paper introduces a power-efficient readout scheme for CMOS image sensors utilizing SAR ADCs. Inspired by the strong correlation between neighboring pixels, each SAR ADC assigned to readout multiple columns of pixels reads each pixel by first copying several MSBs from the previous pixel and, desirably, converts only LSBs to save conversion cycles and power consumption. The readout concept was proved with a prototype QQVGA CIS implemented in a 0.18um CIS process.

Keywords: SAR ADC, multi-column-parallel, delta-readout