Low-noise CMOS image sensors towards single-photon detection

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Abstract A deep sub-electron read noise and high conversion gain CMOS image sensor using reset-gate-less pixel has been developed and demonstrated for the first time at photoelectron-counting-level imaging. The developed CIS based on a multiple sampling technique has a high conversion gain of 220μV/e- and a low read noise of 0.27e-rms.

Keywords: CMOS image sensors (CISs), low read noise, high conversion gain, photon detection.

1. Introduction

Low-noise imaging devices are the key components behind many of the new and emerging photonics technologies. Single-photon detection at visible and near-infrared wavelengths (in the range 400nm to 1060nm) based on silicon is a relatively mature technology with several efficient devices commercially available. The most CMOS-based imaging device is a single-photon avalanche diode (SPAD) detector [1], [2], which is a solid-state photodetector in which a photon-generated carrier can trigger an avalanche current due to the impact ionization mechanism. In the case of SPADs, however, they need large in-pixel circuits for the pixel implementation, which results in a reduction in the spatial resolution and a relatively small fill factor as well as a limitation on high dark count rate.

In this paper, a CIS with an extremely low noise performance, implemented by a 0.11μm Dongbu HiTeK (DBH) CIS process, is introduced [3]. To do this, a high pixel conversion gain (CG) pixel, named a reset-gate-less (RGL) pixel, has been developed and it is successfully demonstrated by the sensor evaluation. The RGL pixel CMOS image sensor (CIS) achieves a high CG of 220μV/e- and deep sub-single-electron read noise of 0.27e-rms.

2. Architecture of prototype CIS

2.1. Reset-gate-less pixel

Fig. 1(a) shows a block diagram of the entire sensor architecture with RGL pixel array. The sensor consists of a pixel array, column-parallel readout circuits based on correlated multiple sampling (CMS) technique, logic block for digital signal processing, and scanners for vertical and horizontal addressing. The entire pixel array is composed of a RGL pixel array, a conventional low-noise pixel array for comparison with the RGL pixel, and other test pixels (TPs). For supplying the high voltage (3 to 25V) to RGL pixels for a floating diffusion (FD) reset operation, an external reset clock (V_{RT}) is given as global operation as shown in Fig. 1(b). At the same time, to reduce the sensor noise such as a thermal noise component, the analog signals from the pixels are read through the low-noise column-parallel readout circuits [4], which use the CMS technique. In RGL pixel, two techniques are used for achieving the high CG. The first method helps to reduce the parasitic capacitance between the charge transfer gate (TG) and FD node. As placing a fully depleted diode structure between the TG and FD, the coupling capacitance, which is generated between the TG and FD, can be decreased. This is also effective method for reducing the noise components from common power lines. The second method perfectly removes the parasitic capacitance

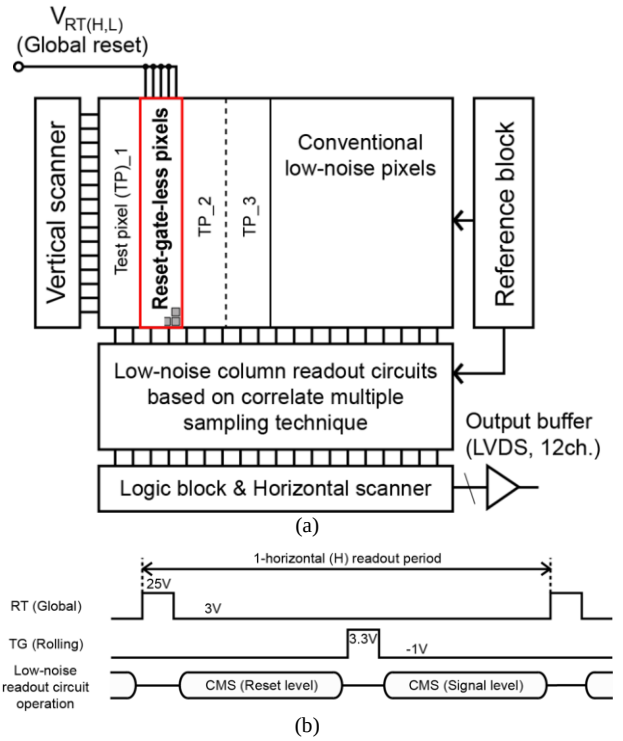

Fig. 1. (a) Chip diagram of developed ultra-low-noise CMOS image sensor with RGL pixel array. (b) Simplified timing diagram (1-horizontal readout cycle).

between the reset gate (RG) and FD because a reset transistor is not used for the proposed pixel. The pixel reset operation is implemented by an implanted n+ layer located close to the FD node. This n+ implant is termed a reset-generating implant (RGI).

Fig. 2 shows the 3-dimensional device simulation results of RGL pixel. The reset barrier between FD and RGI is controlled by the supply voltage to RGI, V_{RT}. During the signal readout period, a low level voltage of 3V is supplied to RGI to make the enough high potential barrier. After reading out the signal from FD node, a high voltage, approximately 25V, is applied to RGI, a reset barrier is lowered. Then a punch-through is occurred between FD and RGI, the FD is reset by a minimum potential level of the lowered reset barrier. Thus, these operations are called as the punch-through reset [5].

2.2. Low-noise readout circuits

Scientific applications of solid-state imagers strongly require very low temporal noise, wide dynamic range, and very high gray scale resolution as well as the optimized pixel structure. A column-parallel analog-to-digital converter (ADC) in CIS is one

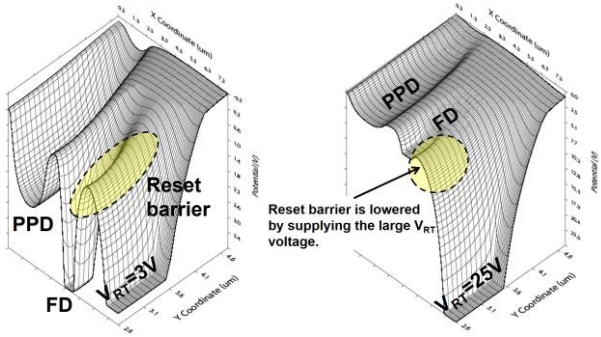

Fig. 2. 3-dimensional potential diagrams of RGL pixel when $V_{RT,L}$=3V (left) and $V_{RT,H}$=25V (right), respectively.

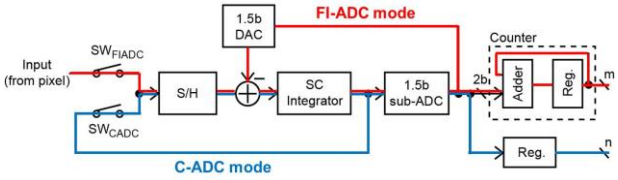

Fig. 3. Block diagram of folding-integration/cyclic ADC.

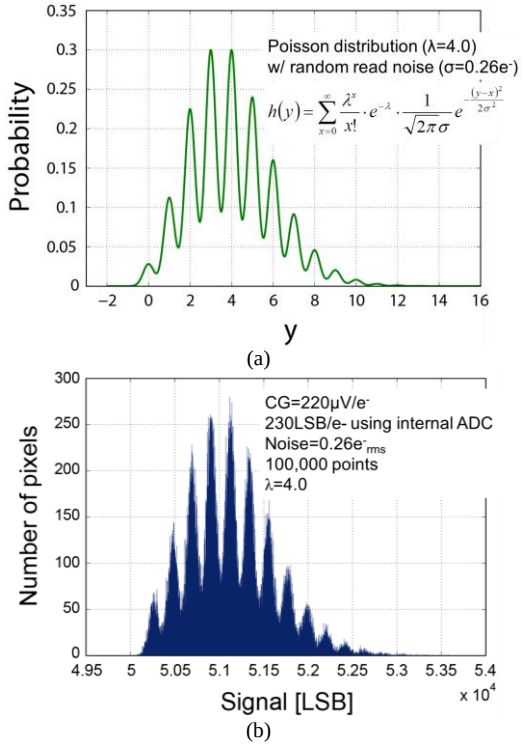

Fig. 4. Photoelectron-counting histogram (PCH). (a) Theoretical Poisson distribution with Gaussian noise. (b) Measured PCH of the RGL pixel CIS (@100,000 points, read noise level=0.26e-rms, mean signal=4e-).

of the important techniques to meet these requirements. Particularly, in case of RGL pixel CIS, the low-noise column-parallel readout circuit is an essential part to achieve single-photon sensitivity. Fig. 3 shows a block diagram of the used column-parallel readout circuit, named a folding-integration /cyclic (FIC) ADC [4]. It consists of an analog core for the ADC, a digital counter for the FI-ADC and a register for C-ADC. The analog core is used for both the FI and C-ADC. It is composed of a switched-capacitor (SC) amplifier, two capacitors, two comparators for a 1.5b sub-ADC, and a 1.5b digital-to-analog converter (DAC) for reference subtraction.

Briefly, in the FI-ADC mode, the pixel outputs are sampled

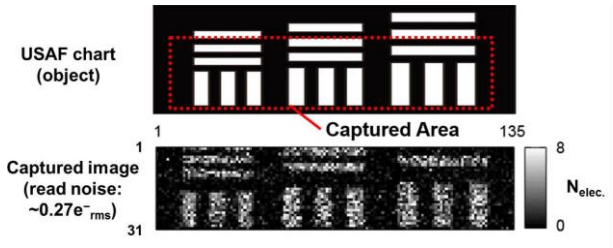

Fig. 5. Captured image (@Target object: USAF test chart, analog gain: 128 times).

multiple (M) times and the sampled signals are integrated over in the SC integrator after the reset operation for initialization which enables the precise digital correlated double sampling (CDS) by eliminating an input dependence of the settling error resulting from the residual charges in a short sampling period. And then the amplified and folded analog output is converted to digital in the C-ADC mode.

3. Measurement results

Fig. 4 shows the photoelectron-counting histogram (PCH) of the RGL pixel CIS with a theoretical Possion distribution (λ=4.0). To attain the PCH, a particular pixel is saved several times (100,000 points) with the 19b column ADC. The measured result is almost the same as the theoretical Poisson distributions with a Gaussian noise distribution. The valley-to-peak modulations of PCH indicate the read noise level of 0.26e-rms, and the exact pixel CG can be calculated from the measured PCH distribution, in this case, 220μV/e-.

Fig 5 shows the captured image with the USAF test chart for demonstrating the photon-counting capability of the developed RGL pixel CIS. This is first proof of the photon-counting-level image using the low-noise CIS without avalanche gain.

4. Conclusion

An extremely low-noise CIS with RGL pixels using a standard 0.11 DBH CIS process is developed. The high contrast image captured by the CIS, which has less than 0.3e-rms noise level, has been shown at a very low light condition of less than eight electrons per pixel. This suggests that photon-counting-level imaging can be realized, and the developed photon-countable sensitivity CIS is suitable for many scientific and industry applications that require both single-photon sensitivity and sufficient dynamic range.

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References

[1] P. Seitz and A. J. P .Theuwissen, Single-Photon Imaging. New York, NY, USA: Springer-Verlag, 2011.

[2] N. A. W. Dutton et al., in Symp. VLSI Circuits Dig. Tech. Papaers, Jun. 2014.

[3] M.-W. Seo et al., EDL, 36(12), pp. 1344-1347, Dec. 2015

[4] M.-W. Seo et al., JSSC, 47(1), pp. 272-283, Jan. 2012.

[5] M. Guidash, U.S. Patent 5872371, Feb. 16th, 1999.