A dead-time free global shutter stacked CMOS image sensor with in-pixel LOFIC and ADC using pixel-wise connections

Rihito Kuroda, Hidetake Sugo, Shunichi Wakashima, and Shigetoshi Sugawa
Graduate School of Engineering, Tohoku University
6-6-11 Aza-Aoba, Aramaki, Aoba-ku, Sendai, 980-8579 Japan
E-mail: rihito.kuroda.e3@tohoku.ac.jp

Abstract An almost 100% temporal aperture (dead-time free) global shutter (GS) stacked CMOS image sensor with in-pixel lateral overflow integration capacitor (LOFIC), ADC and DRAM using pixel-wise connections is presented. The structure, operation and the measurement result of the fabricated prototype chip are summarized.

Keywords: CMOS image sensor, global shutter, pixel-wise connection, LOFIC

1. Introduction

The global shutter (GS) function is strongly required in many application fields to capture fast moving objects without image distortion. In order to implement the GS function into CIS, pixel signal must be temporally stored until sequential readout. There are several types of GS CIS classified by the domain of the signal storage; the photo-charge storage type with charge storage node and two-stage charge transfer function [1-3] and with floating diffusion (FD) as storage [4], the signal voltage storage type [5-6], and the digital signal storage type with in-pixel ADC [7-8]. In addition to the high shutter efficiency and high frame rate, a wide dynamic range performance and 100% temporal aperture (dead-time free) are important performances required in GS image sensors. Regarding the high shutter efficiency and noise performances, the in-pixel ADC with digital signal storage is attractive [7-8], however achieving a high aperture ratio has been a challenge. In order to achieve the in-pixel ADC with a small pixel size, 3D stacking technology is to be useful [6, 9].

This work presents a back side illumination (BSI) stacked CIS with in-pixel lateral overflow integration capacitor (LOFIC), single slope (SS) ADC and DRAM, enabled by pixel-wise connections [11]. To develop a scalable architecture and achieve a low power consumption and a wide dynamic range, the charge domain dynamic range extension with LOFIC [10], and 1.2V V_{DD} 65nm technology-node transistors for in-pixel ADC and DRAM were simultaneously introduced.

2. Developed CMOS Image Sensor

Fig.1 shows the structure of the developed stacked CIS. It consists of a BSI PD substrate with an array of PDs and pixel transistors including LOFIC and an ASIC substrate with an array of in-pixel ADCs, DRAM and sensing amplifier/repeater circuit, row selector, pipeline SRAM, and horizontal shift resistor (HSR) and output buffers. The two substrates are stacked with pixel-wise connections. The two operation modes are implemented in the developed sensor; 6.6μm-pitch VGA pixel dead-time free GS mode with wide dynamic range enabled by LOFIC, and 1.65μm-pitch 4.9M sub-pixel high resolution rolling shutter (RS) mode. Using a more miniaturized technology-node for ASIC substrate, the pixel pitch is to be further scaled down. Fig.2 shows the schematic and layout diagrams of pixel circuit. The PD substrate side consists of FD shared sixteen sub-pixels, LOFIC, reset switch (R), switch between FD and LOFIC (S), source follower (SF), current source (CS) and CS control switch (X). The LOFIC is employed to resolve the trade-off between conversion gain and FWC by generating high conversion gain signal with C_{FD} and high FWC signal with C_{FD}+C_{LOFIC} using overflow photoelectrons under a single exposure [10]. The ASIC substrate side consists of a 12bit SS ADC and four 12bit 3T-DRAM cells and signal selection switches to select high conversion gain signals (N1 and S1) and high FWC signals (N2 and S2), respectively. The SF output and ADC input were connected by pixel-wise connections. The LOFIC structure captures a wide dynamic range signals by the charge domain, thus, the small voltage swing is sufficient. The power supply voltages for PD and ASIC substrates are 3.3V and 1.2V, respectively. A column 12bit data I/O lines are used for both writing and reading operations of DRAM. In each bit line, a sensing amplifier/repeater circuit composed of a set of a CMOS buffer and a switch is placed in every twelve rows in order to achieve a high speed writing and reading operations [11]. Fig.3 shows the pulse timing diagram for GS and RS operation modes. In GS mode, four kinds of pixel signals for wide dynamic range operation are digitized and stored in DRAMs until readout during the exposure period of next frame. The exposure and the readout are carried out simultaneously, thus the dead-time free integration is achieved. In the RS mode, during each row selecting period, N1 and S1 of sub-pixels 1 are digitized, stored and readout. Then, sub-pixels 2 through 16 sequentially operate in the same manner. Fig.4 shows the micrograph of the fabricated sensor chip and the digital camera system. Fig.5 shows the captured sample images obtained by GS mode. A distortion-free, dead-time free image by high CG and high FWC signals is captured. Table 1 shows the performance summary of the chip. The FWC was 220ke$^-$ in GS mode with linear response. In GS mode the temporal aperture ratio becomes 99% at 120fps.

3. Conclusion

A stacked CIS with in-pixel LOFIC, 12bit SS ADC and DRAM with dead-time free wide dynamic range GS mode and high resolution RS mode was developed using pixel-wise connections. A sample image capturing was demonstrated by the prototype chip fabricated with a 45nm 1P4M CIS technology for PD substrate and a 65nm 1P5M CMOS technology for ASIC substrate. An advanced GS function with scalable architecture was developed by the 3D stacking technology.

Acknowledgments

The authors would like to thank TSMC CIS teams for their technical support.

References

[1] K. Yasutomi, S. Itoh, S. Kawahito: "A 2.7e$^-$ Temporal Noise 99.7% Shutter Efficiency 92dB Dynamic Range CMOS Image Sensor with Dual Global Shutter Pixels", 2010 ISSCC, Dig. Tech. Papers, pp.398-399 (Feb. 2010)

[2] M. Sakakibara, Y. Oike, T. Takatsuka, A. Kato, K. Honda et al: "An 83dB-Dynamic-Range Single-Exposure Global-

Shutter CMOS Image Sensor with In-Pixel Dual Storage", 2012 ISSCC, Dig. Tech. Papers, pp.380-381 (Feb. 2012)
[3] Y. Oike, K. Akiyama, L.D. Hung, W. Niitsuma, A. Kato, M. Sato et al: "An 8.3M-pixel 480fps Global-Shutter CMOS Image Sensor with Gain-Adaptive Column ADCs and 2-on-1 Stacked Device Structure", 2016 Symp. VLSI Circuits, Dig. Tech. Papers, pp.222-223 (June 2016)
[4] M. Takase, Y. Miyake, T. Yamada, T. Tamaki, M. Murakami and Y. Inoue: "First demonstration of 0.9 μm pixel global shutter operation by novel charge control in organic photoconductive film", 2015 IEDM Tech. Dig., pp.775-778 (Dec. 2015)
[5] G. Meynants, J. Bogaerts, X. Wamg, G. Vanhorebeek: "Backside illuminated global shutter CMOS image sensors", Proc. Intl. Image Sensor Workshop, pp.305-308 (June 2011)
[6] T. Kondo, Y. Takemoto, K. Kobayashi, M. Tsukimura, N. Takazawa, H. Kato et al: "A 3D stacked CMOS image sensor with 16Mpixel global-shutter mode and 2Mpixel 10000fps mode using 4 million interconnections", 2015 Symp. VLSI Circuits, Dig. Tech. Papers, pp.C90-C91 (June 2015)
[7] S. Kleinfelder, S. Lim, X. Liu, A.E. Gamal: "A 10 000 Frames/s CMOS Digital Pixel Sensor", IEEE J. Solid-State Circuits, **36**, 12, pp.2049-2059 (2001)
[8] T. Komuro, S. Kagami, and M. Ishikawa: "A Dynamically Reconfigurable SIMD Processor for a Vision Chip", IEEE J. Solid-State Circuits, **39**, 1, pp.265-268 (2004)
[9] M. Goto, K. Hagiwara, Y. Iguchi, H. Ohtake, T. Saraya, M. Kobayashi, E. Higurashi, and T. Hiramoto: "Three-Dimensional Integrated CMOS Image Sensors with Pixel-Parallel A/D Converters Fabricated by Direct Bonding of SOI Layers", 2014 IEDM Tech. Dig., pp.84-87 (Dec. 2014)
[10] N. Akahane, S. Sugawa, S. Adachi, K. Mori, T. Ishiuchi and K. Mizobuchi: "A Sensitivity and Linearity Improvement of a 100-dB Dynamic Range CMOS Image Sensor Using a Lateral Overflow Integration Capacitor", IEEE J. Solid-State Circuits, **41**, 4, pp.851-858 (2006)
[11] H. Sugo, S. Wakashima, R. Kuroda, Y. Yamashita, H. Sumi, T.J. Wang, P.S. Chou, M.C. Hsu and S. Sugawa: "A Dead-time Free Global Shutter CMOS Image Sensor with in-pixel LOFIC and ADC using Pixel-wise Connections", 2016 Symp. VLSI Circuits, pp.224-225 (June 2016)

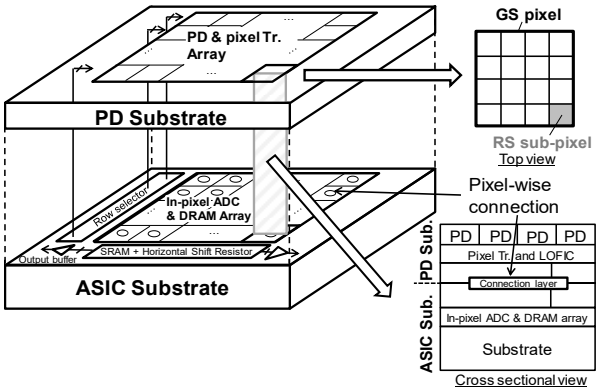


Fig.1 Structure of developed CIS.

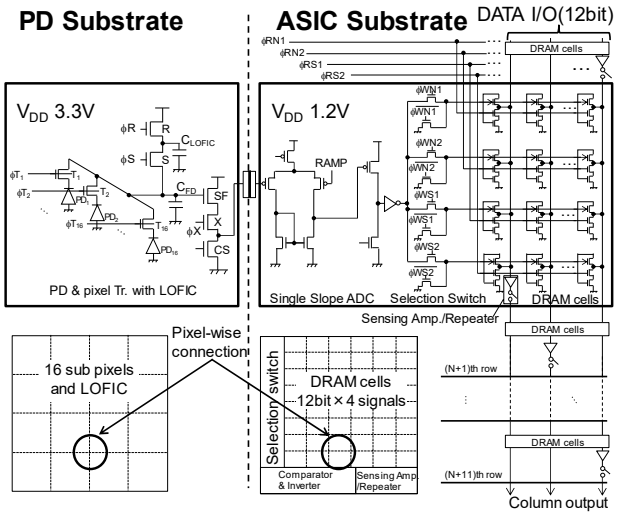
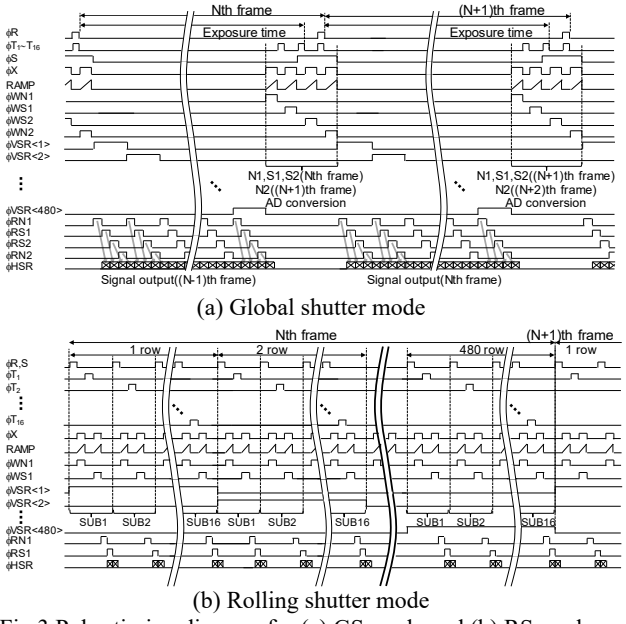


Fig.2 Pixel circuit schematic and layout diagrams.



(a) Global shutter mode

(b) Rolling shutter mode

Fig.3 Pulse timing diagram for (a) GS mode and (b) RS mode.

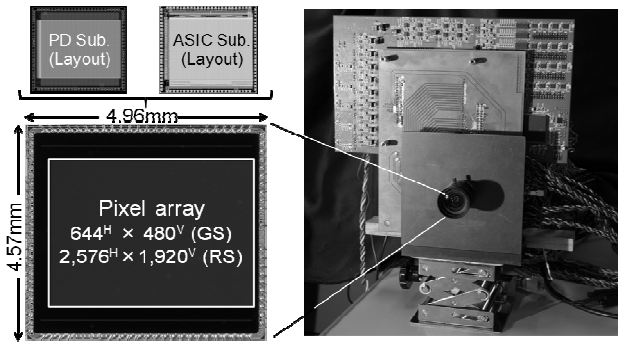


Fig.4 Chip micrograph (left) and digital camera system (right).

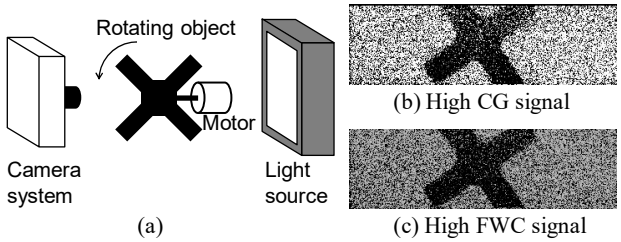


Fig.5 (a) Schematic illustration of the sample image capturing and captured images using the GS mode, (b) high CG signal and (c) high FWC signals. A part ($320^H \times 94^V$) of the full pixel region is shown.

Table 1 Performance summary.

Fabrication. Process (PD die / ASIC die)	45nm 1P4M CMOS / 65nm 1P5M CMOS	
Chip size	$4{,}960\mu m^H \times 4{,}570\mu m^V$	
# of pixels (GS mode/ RS mode)	Total	$644^H \times 480^V$ / $2{,}576^H \times 1{,}920^V$
	Effective	$640^H \times 476^V$ / $2{,}560^H \times 1{,}904^V$
Pixel pitch (GS mode/ RS mode)	6.6μm / 1.65μm	
# of connection per pixel	1 connection / pixel (GS mode)	
Shutter mode	GS / RS	
ADC type	12bit, Single Slope in pixel ADC	
Pixel Memory	12bit × 4 channel	
VDD (PD sub. / ASIC sub.)	3.3V / 1.2V	
Full Well Capacity (GS mode)	220ke-	
Integration dead-time per frame	80μs (time aperture ratio: 99% @ 120fps)	