3D-stacking architecture for low-noise high-speed image sensors

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Abstract In this paper, architectures for low-noise high-speed image sensors based on 3D stacking technology are discussed. Effectiveness of the 3D-stacking technology for low-noise high-speed image sensors is demonstrated in an implementation of a 33Mpixel 240fps 3D-stacked CMOS image sensor based on 12b 3-stage cyclic-based pipelined ADCs. For extremely low noise and wide dynamic range imaging, highly-parallel multiple-sampling based ADC will be an important technique for 3-D stacked CMOS image sensors.

Keywords: noise reduction, multi-aperture, random telegraph signal noise, dark current

1. Introduction

3D-stacking LSIs integrating imaging pixels have been developed since 1980's for demonstrating the advantage of the 3D-stacking LSI technology [1][2]. Recently, the 3D-stacking technology for image sensors is revived and it is becoming an inevitable technology for present and near future CMOS image sensors [3][4]. The 3D-stacking technology has a distinct merit for realizing image sensors with advanced performance on noise, speed, dynamic range, power consumption and functionality. On the other hand, a viewpoint from the circuit and device technology suitable for 3D-stacking integration is also very importance. The recently reported 33Mpixel 240fps CMOS image sensor which consumes 3W [3] is successfully developed thanks to the 3D-stacking technology with high-density via connections and a new ADC architecture using a 3-stage cyclic-based ADC. In this article, ADC circuit technologies suitable for 3-D stacking integration is discussed. The basic ADC architectures of interest here are the cyclic-based ADC and multiple-sampling based ADC.

2. 3D-stacked cyclic-based ADC for 8K imagers

Figure 1 shows a 3-dimensional illustration of the backside-illuminated 3D-stacked 33Mpixel/240fps CMOS image sensor [4]. The pixel wafer has a total of 9,600(H)×5,396(V) with 1.1μm-pitch 2×2-shared pixels. The effective pixel array is 7,728(H)×4,368(V) for 33Mpixel/240fps mode. The ASIC wafer of the chip has a 1,932(H)×4(V) CDS/ADC array with a 12b 3-stage cyclic based ADC architecture. Each 4 sets of 2×2-shared pixels share output lines and connect with 4 CDS/ADCs. There are a total of 20 blocks of horizontal scanners, current-mode logic (CML) circuits, digital processing circuits, SLVS drivers. Each block has 6-fold parallel 1.2Gb/s SLVS output ports; therefore, in total 120 ports output an aggregate data rate of 144Gb/s. In the previous work [5], a two-stage pipelined operation of the first 4b and second 8b cyclic ADCs was applied to a 33Mpixel 120fps CMOS image sensor, and its high efficiency for high-speed low-power operation was demonstrated. The three-stage ADC with cyclic/cyclic/SAR pipelined stages in this implementation realizes 240fps operation while maintaining low power and low noise. The 3-stage cyclic-based ADC, and it was 120μW while realizing a conversion time period of 0.92μs. The layout area of the 3-stage cyclic-based ADC is 4.4μm (H) × 920μm (V), which enables the placing of 4 CDS/ADCs along the column direction. The maximum measured differential nonlinearity (DNL) and integral nonlinearity (INL) is +0.82/-0.88 LSB INL is +1.04/-11.75 LSB, which is within 0.31% of the signal full-scale range. The pixel wafer of the chip is fabricated using a 45 nm 1P4M MOS process, and the ASIC wafer of the chip is fabricated using a 65 nm 1P5M logic process. The image size is 8.448mm(H)× 4.752mm(V). The sensitivity is 0.55V/lx-s without a color filter and micro lens, and full-well capacity is 5,700e-. Random noise of 3.6e-$_{rms}$ is obtained at an analog gain of 4.0 and a pixel rate of 7.96Gpixel/s. The total power consumption is 3.0W.

3. 3D-stacked multiple-sampling-based ADC

For ultra-low-noise imaging, a pixel device and circuit for high conversion gain and high-gain readout circuits are essential.

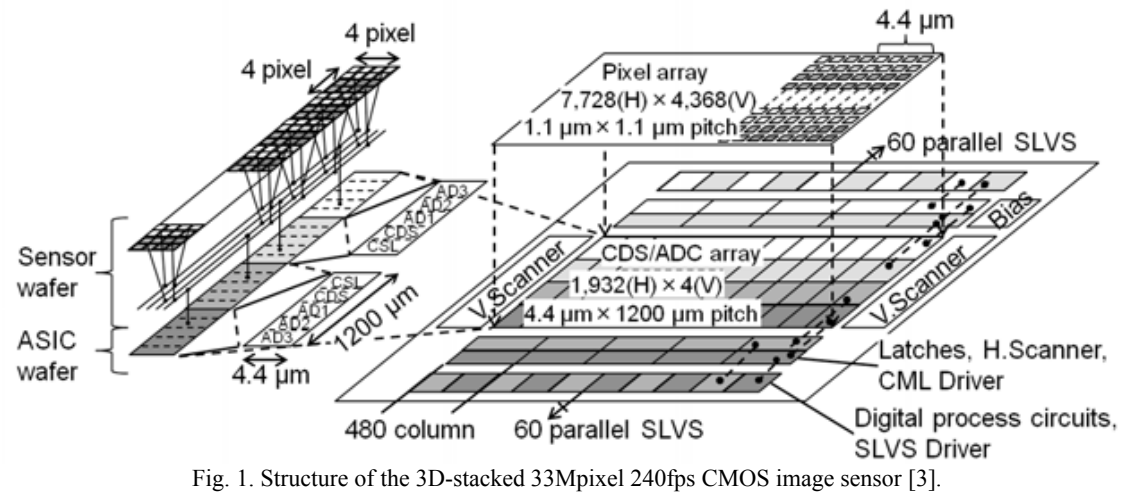


Fig. 1. Structure of the 3D-stacked 33Mpixel 240fps CMOS image sensor [3].

A pixel parallel or block parallel (consisting of several pixels) ADC using multiple-sampling technique will be an important technology in the near future for realizing extremely low-noise which enables photo-electron counting, sufficient dynamic range, and reasonable frame rate. Such a high-performance ADC requires large circuit volume for both analog and digital circuits, but by using 3D-stacking with 3 layers as shown in Fig. 2, an ADC using multiple sampling technique based on pixel-parallel or block parallel (with several pixels) architecture will be realized. Fig. 3 shows an example of the circuit and block diagram of the multiple-sampling based ADC. In this ADC, the folding-integration (FI) ADC which works as a resettable delta-sigma modulator performs the multiple sampling of the pixel output and very high gain is applied for reading the signal, resulting in a very small input-referred noise. The extended conversion is performed by a cyclic ADC mode of operation using the same analog core circuits as those for the FI ADC. Because of the negative feedback of the modulation loop of the FI ADC, the amplitude of the amplifier is suppressed within a linear range and hence this ADC has a wide dynamic range and high gray-scale resolution. Though the ADC occupies relatively large area if it is implemented at the column of CMOS imagers, the area must be reduced by choosing very small active device and passive component sizes. The choice of such small device/component sizes leads to the increase of noise, pixel-to-pixel deviation and non-linearity of A/D conversion. However, these problems can be overcome by using very large sampling number and digital domain processing for error correction. Fig. 4 shows an example of read noise calculation for the case of column parallel implementation of the FI/cyclic ADC [6]. Using very high gain (>128), the noise components other than the flicker noise (1/f noise) during the pixel sampling can be negligibly small, and therefore, the choice of very aggressively small deice and passive-component sizes in the ADC can still maintain very small total noise. The problems of the pixel-to-pixel variation and the non-linearity can be recovered by using digital domain error correction techniques.

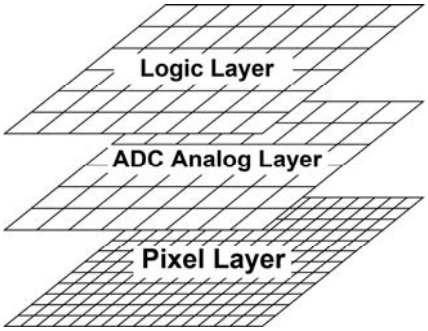
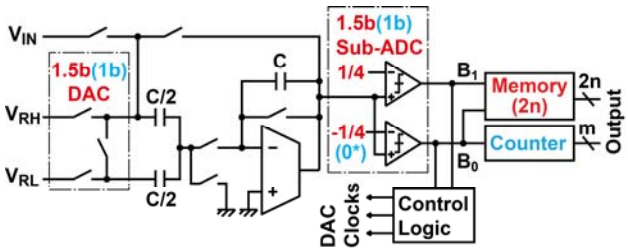
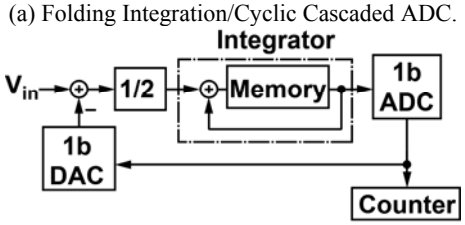


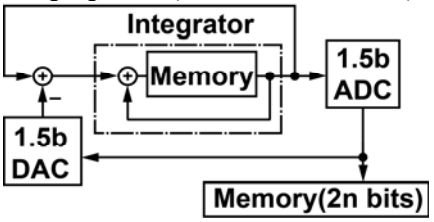
Fig. 2.3D-stacked (3Layers) CMOS image sensor.



(a) Folding Integration/Cyclic Cascaded ADC.



(b) Folding Ingeration (Resettable ΔΣ moulator) mode.



(c) Cyclic ADC mode.

Fig. 3. Block Diagram of the multiple-sampling based ADC.

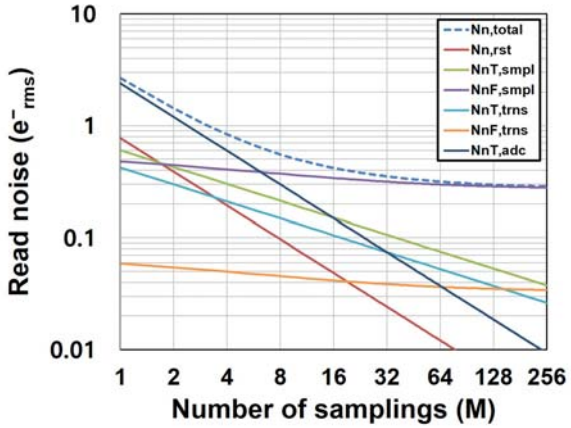


Fig. 4. Calculated read noise of CIS using multiple-sampling based ADC (*Nn,rst*:reset noise of column SC amp. , $N_{T/F}$, *smpl*: pixel sampling noise (T:thermal, F:flicker), $N_{T/F}$, *trns*: SC amp. noise in charge transfer phase, $N_{T/,ADC}$: noise of cyclic ADC [6].

5. Conclusion

ADC architectures suitable for 3D-stacking implementation is discussed. Multiple-sampling-based ADC will be an important technology, but the demonstration of the ADC with very high performance even with very small transistor /component sizes is necessary, which is left as a near future subject.

Acknowledgments

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