A High-speed Low-power CMOS Image Sensor with Delta and Interpolation Readout Scheme

Hyeon-June Kim, Sun-Il Hwang, and Seung-Tak Ryu
School of Electrical Engineering, KAIST
291 Daehak-ro Yuseong-gu, Daejeon, 34141 Republic of Korea

E-mail: kaist3191@kaist.ac.kr

Abstract

This paper presents a high-speed low-power readout scheme for CMOS image sensors (CISs) that utilizes the image properties. The proposed delta and interpolation readout (DI-readout) scheme reads the signal difference between two adjacent pixels (Δpixel) by utilizing MSBs information of the previous pixel, using large Δpixel for interpolation and small Δpixel for delta readout. By effectively reducing the dynamic range of the signal, the proposed readout scheme can reduce the number of decision cycles and the power consumption of SAR ADC. A prototype QQVGA CIS with ten 10-bit SAR ADCs was fabricated in a 0.18 μm 1P4M CIS process with a 4.4 μm pixel pitch. The measurement results of the implemented prototype CIS showed a figure-of-merit (FoM) for imager of 0.35 e-nJ.

Keywords: Low power, high speed, delta, pseudo-interpolation, SAR ADC, multi-column-parallel, delta-readout

1. Introduction

In recent years, the emergence of high-performance CMOS image sensors (CISs) has been enlarging in the imager market. In particular, for personalized mobile devices powered by batteries, such as mobile phones and tablet PCs, a low-power CIS design is essential. Also, the pixel rate of some applications such as industrial high speed machine vision sensors is becoming faster as their pixel resolution and frame rate increase. Especially, the increased pixel resolution makes it difficult to meet the required reporting rate of image processing for edge extraction in specific applications such as auto-focusing and machine vision devices.

Thus far, most efforts to improve the operating speed and reduce the power consumption of CISs have been focused on circuit-level approaches. Recently, beyond the circuit-level, a delta readout scheme (D-readout) [1] with which pixel data is read according to the difference from the adjacent pixel (delta, Δ_{pixel}) has been proposed for a power-reduced readout along with SAR ADCs in CIS. By resolving only the remaining LSBs after copying the MSBs from the previous pixel, the number of conversion cycles can be reduced, resulting in a power reduction. In large Δ_{pixel} cases at the edges of an object in an image, however, because the normal SAR conversion should be considered, the readout speed is reduced rather than the traditional SAR.

In this work, we propose a Delta and Interpolation (DI) Readout scheme that operates in two readout modes: Delta-readout for small Δ_{pixel} and pseudo-interpolation (PI) readout for large Δ_{pixel}. Unlike the case in [1], because the PI-readout scheme can cover large Δ_{pixel}s with the same amount of operation time as D-readout for small Δ_{pixel}s, the proposed scheme can reduce operation clock cycles resulting in high speed performance. Considering that large Δ_{pixel}s exist mostly at the edges of objects in an image, the results of the PI-readout can be utilized as the edge information. Thus we can additionally obtain edge maps with high speed images at the same time, while maintaining the low power performance without any image processing.

2. Proposed Readout scheme

The timing diagrams of 10-bit SAR ADC operation with the D-readout algorithm[1] and the proposed DI-readout algorithm are shown in Fig. 1. In the D-readout algorithm, after 5-bit MSB copying and D-window checking ($T_{1\text{-}3}$), a full 10-bit A/D conversion is performed for large Δ_{pixel}s during $T_{4\text{-}14}$. For small Δ_{pixel} cases, however, A/D conversion is completed by resolving only the remaining LSB codes, so the time period from T_8 to T_{14} is redundant. On the other hand, the proposed DI-readout algorithm can improve not only the power efficiency of SAR ADC, but also its conversion speed. In cases of large Δ_{pixel}, the PI-readout performs with the same amount of operation time as that of the D-readout for small Δ_{pixel}s ($T_{4\text{-}7}$). Therefore, only 7 cycles are needed, even for large Δ_{pixel} cases; consequently, the overall process enhances readout speed by around 50%.

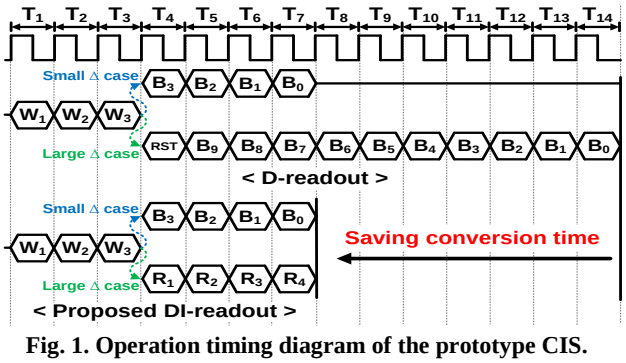


Fig. 1. Operation timing diagram of the prototype CIS.

A schematic diagram of the proposed DI-readout SAR ADC is shown in Fig. 2. PI-DAC was added to CDAC, which is composed of 4 capacitors of 16C each. The capacitance of the PI-DAC was chosen using an estimation of the trade-off between the error rate and the hardware complexity. Even with those considerations, output images can be blurred by the PI-readout. However, the effect of the PI-readout can be lowered by the low

occurrences of large Δ_{pixel} and the averaging effect of the human-eye. Also, this process is more effective in higher pixel resolution CIS.

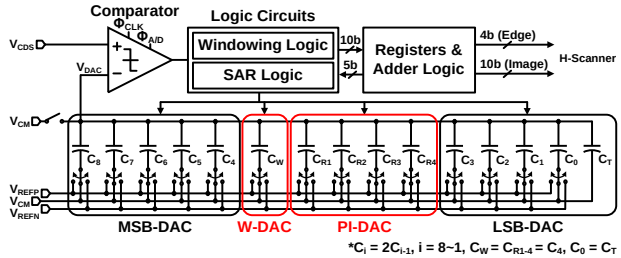


Fig. 2. Schematic diagram of the 10-bit SAR ADC used for the proposed DI-readout scheme

A CDAC waveform of the proposed DI-readout SAR ADC in a large Δ_{pixel} case is shown in Fig. 3. For the pixel P[j], after voltage generation of the CDAC by the 5-bit MSB codes of the previous pixel P[j-1] (V_{CDAC}), and D-window checking, the PI-readout starts. At each phase, CDAC switching is performed at 16LSB (1LSB size of 5-bit MSB) and the comparator checks whether the input signal exists within the switching range or not. Since the results of the PI-readout include edge information of the image, edge maps can be simply obtained by the image sensor with the proposed scheme. With these edge maps, post-image processing for applications such as machine vision, object recognition, and auto-focusing can be more efficient because edge extraction of the ISP is unnecessary. In addition, with the edge codes R_{1-4} for the 4-level threshold voltages (V_{TH1-4}), 4 types of edge map can be obtained at the same time; these maps are applicable to the control of the magnitude of the edges.

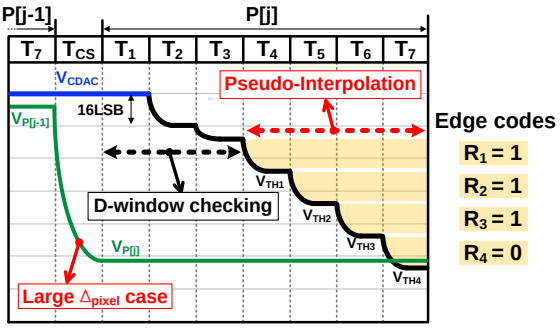
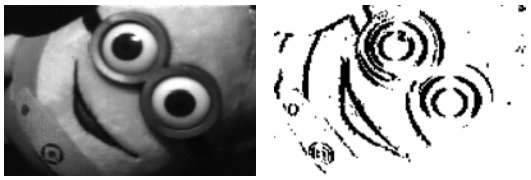


Fig. 3. CDAC waveform of the 10-bit SAR ADC used for the proposed DI-readout scheme in a large Δ_{pixel} case.

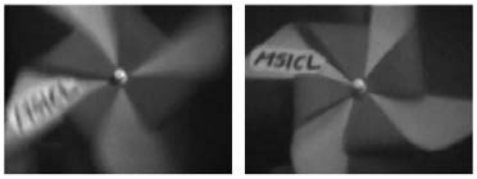
3. Experimental Results

The prototype image sensor is fabricated in a 1P4M 0.18 μm CIS process. A 160 × 120 array of 4.9 μm-pitch 4T-APS pixels is implemented. The sample image and its edge image captured by the prototype chip are shown in Fig. 4. Also, to demonstrate the sensor's high-speed performance, sample images captured at 1,500 fps and 3,200 fps are shown in Fig. 5. The measured temporal noise is 5 e^-_{rms} and the power consumption is 4.3 mW. The figure-of-merit (FoM) of the various ADC types, calculated by (1) as denoted in [2], is plotted in Fig. 6. The prototype image sensor shows an FoM of 0.35 e-nJ at 3,200 fps, which is state-of-the-art performance in Group A. In addition, the estimated FoMs at pixel rates of 737 Mpixel/sec (Group B) and 2.95 Gpixel/sec (Group C) are 0.56 e-nJ and 0.9 e-nJ, respectively, which are also state-of-the-art performances.



(a) (b)

Fig. 4. Sample image taken from the prototype CIS: (a) original image and (b) edge image.



(a) (b)

Fig. 5. Sample image taken from the prototype CIS: (a) at 1,500 fps and (b) at 3,200 fps

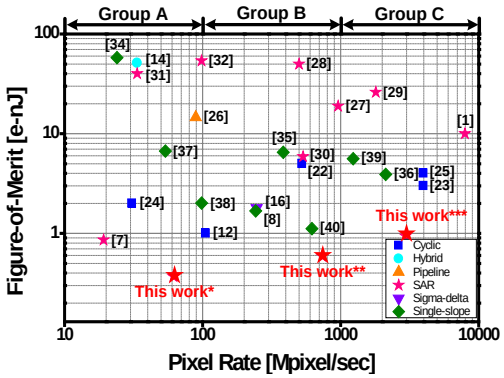


Fig. 6. Figure-of-Merit; *FoM at 61.4 Mp/s, **estimated FoM at 737 Mp/s, and ***estimated FoM at 2.95 Gp/s.

$$FoM = \frac{Power \cdot Noise}{Pixel\ rate} \times 10^9 [e^- \cdot nJ] \quad (1)$$

4. Conclusion

In this paper, an image-dependent speed enhancing and power-saving CIS readout scheme, called the DI-readout scheme, was introduced. In case of large Δ_{pixel}, the DI-readout scheme increases the readout speed using a pseudo-interpolation readout scheme instead of full A/D conversion. The generated edge codes can also be used for post-image processing. The proposed DI-readout scheme can be a promising solution for those attempting to realize high-speed and low-power CISs.

Acknowledgement

This work was supported by the IT R&D program of MOTIE/KEIT. (10049270, SoC-SW platform for computer-vision based UI/UX on wearable smart devices).

References

[1] H. J. Kim *et al.*, "Delta readout scheme for image-dependent power savings in a CMOS image sensor with multi-column-parallel SAR ADCs," in IEEE ASSCC, 2015, pp. 1-4.

[2] S. Kawahito, "Column readout circuit design for high speed low noise imaging," presented at the IEEE ISSCC Image Sensor Forum, San Francisco, CA, Feb. 2010.