Wide dynamic range CMOS image sensor based on dual exposure technique using averaging circuits

Sang-Hwan Kim[1], Byoung-Soo Choi[1], Myunghan Bae[1], Jimin Lee[1], Chang-Woo Oh[2], and Jang-Kyoo Shin[1]
[1]School of Electronics Engineering, Kyungpook National University
80 Daehak-ro, Buk-gu, Daegu, 41566, Korea
[2]Department of Sensor and Display Engineering, Kyungpook National University
80 Daehak-ro, Buk-gu, Daegu. 41566, Korea
E-mail: jkshin@ee.knu.ac.kr

Abstract In this paper, an averaging circuits using dual exposure technique for extending dynamic range of CMOS image sensor is proposed. The proposed CMOS image sensor has been implemented by a chip which is consisted of a pixel array, scanners, and proposed averaging circuits. Despite the equal number of transistors in pixels, it is possible to extend dynamic range of CMOS image sensor by using averaging circuit. In addition, comparing with conventional 3-transistor CMOS image sensor, it was demonstrated that dynamic range is improved from 70dB to 90dB after using average circuit by experimentally. The designed circuit has been fabricated by using 0.18μm 1-poly 6-metal standard CMOS process, and its characteristics are simulated and measured.

Keywords: CMOS image sensor, wide dynamic range, dual exposure, averaging circuit

1. Introduction

Recently in image sensor system, many techniques are using to improve dynamic range of CMOS image sensor. To improve the dynamic range of image sensor is an important performance factor in applications [1-3]. There are several methods to improve dynamic range about image sensor such as extending a photodiode active area, using dual exposure technique, linear-logarithmic (Lin-Log) technique [4].

First, extending the area of photodiode in order to improve the dynamic range has a chip area limit. Secondly, dual exposure technique which captured with different integration time has complex signal processing circuit. Finally, linear-logarithmic (Lin-Log) technique by improving the dynamic range to approximately 120dB by using log property at high illumination condition also using linear property at low illumination condition has advantage but logarithmic pixel has inferior output swing. In addition, this method has a disadvantage in decreasing fill factor of the image sensor by adding more transistor in pixel structure [5-8].

In this paper, we propose an averaging circuit using dual exposure technique for extending dynamic range of CMOS image sensor. CMOS image sensor has been implemented by a chip which is consisted of a pixel array, scanners, and proposed averaging circuits. In addition, averaging circuit performs that combines a voltage signal resulted by performing controls the odd-row and even-row of exposure time. As a result, not only extending dynamic range but controlling sensitivity. The proposed signal processing circuit has been designed and simulated using 0.18μm 1-poly 6-metal standard CMOS process.
.

2. Signal processing and operation

Fig. 1 shows a whole CMOS image sensor block diagram including proposed signal processing circuit. Block diagram is composed of 3-transistor pixel array, odd-vertical scanner, and even-vertical scanner, double sampling circuit, horizontal scanner, and proposed signal processing circuit. The signal output comes after double sampling and proposed signal processing circuit with averaging circuit.

A conventional 3-transistor pixel structure is implemented in this structure and shown Fig. 2. 3-transistor pixel structure consists of M1 reset transistor, M2 source follower transistor, M3 select transistor, M4 bias transistor. Signal electron is converted to voltage by source follower transistor and transmitted to double sampling circuit.

Fig. 3 shows schematic of proposed signal processing circuit. Col(x) and Col(x+1) are column even and odd output after double sampling circuit respectively. Col(x) and Col(x+1) are output signals from a specific column after double sampling. S1 switch turn on when signal voltage of first frame signal in Col(x) and store at capacitor C. After than next frame signal is stored at capacitor C. when turn on S2 switch. Finally, S3 switch trun on so averaging between previous frame signal output and next frame signal output. Buffer circuit consists of PMOS source follower for output signal voltage. After that, each column S4, S5 switches turn on to get final output output signal voltage respectively.

3. Experimental result and conclusion

Fig. 4 shows experimental results of image sensor including proposed signal processing circuit. In a conventional mode, the limitation on the dynamic range of the conventional 3-transistor is found to be the result of node capacitance. Comparing with conventional mode 3-transistor image sensor, it is possible to confirm that dynamic range is increased from 70dB to 90dB by averaging circuits and its processing.

4. Acknowledgements

This work was supported by the Center for Integrated Smart Sensors, funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2013M3A6A6073718), the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2012-0062617), Samsung Electronics Co., Ltd., the BK21 Plus project funded by the Ministry of Education, Korea (21A20131600011), and the Integrated Circuit Design Education Center (IDEC) in Korea.

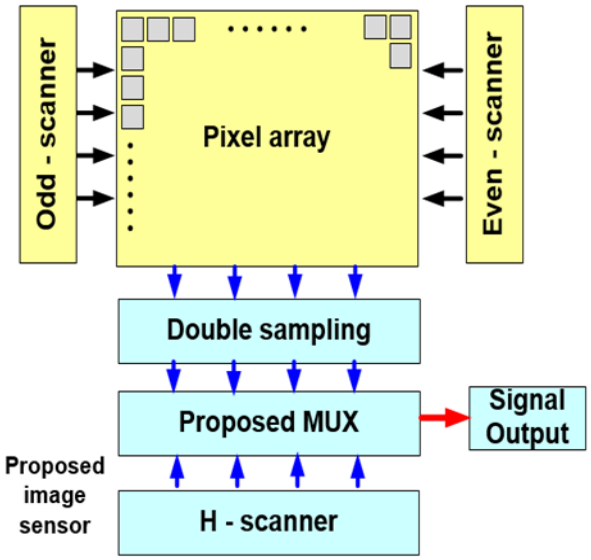

Fig. 1. Block diagram of whole proposed CMOS image sensor.

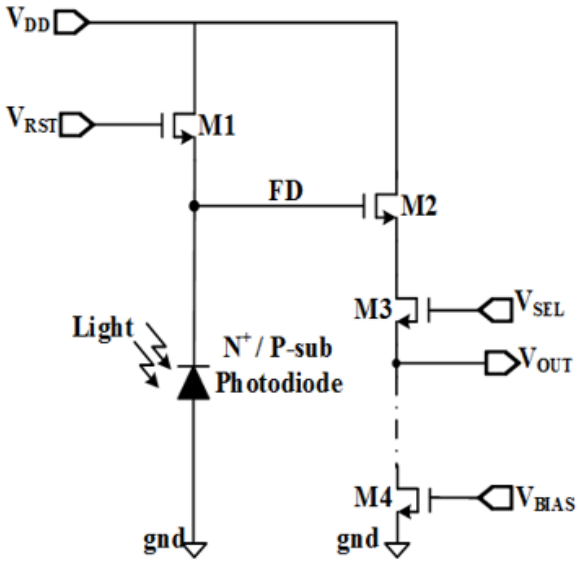

Fig. 2. Schematic of 3-transistor CMOS image sensor.

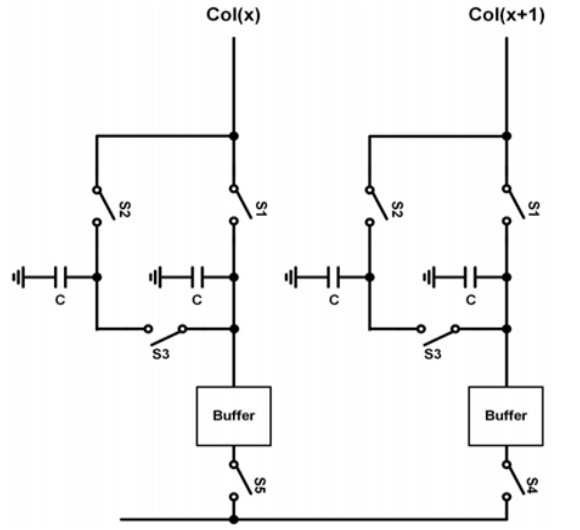

Fig. 3. Schematic of proposed signal processing circuit after double sampling.

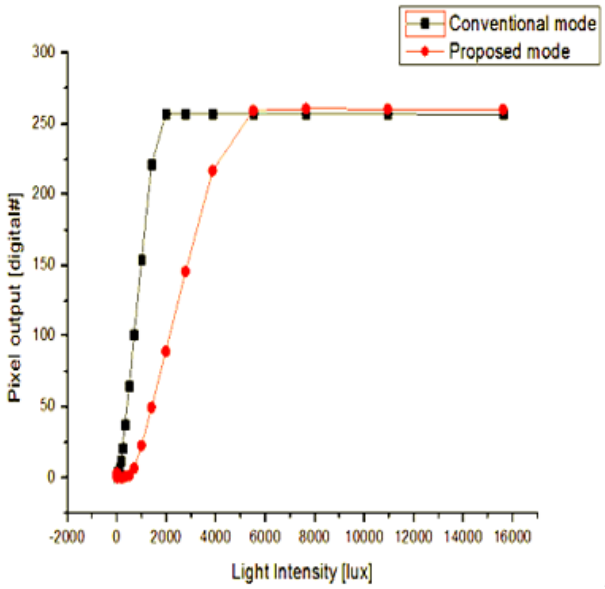

Fig. 4. Experimental result of image sensor including proposed signal processing mode and conventional mode.

References

[1] S. D. Freedman and F. Boussaid, "A high dynamic range CMOS image sensor with a novel pixel-level logarithmic counter memory", *2015 2nd International Conference on Knowledge-Based Engineering and Innovation*, pp. 14-19, 2015

[2] N. Katic, V. Popovic, R. Cojbasic, A. Schmid and Y. Leblebici, "A Relative Imaging CMOS Image Sensor for High Dynamic Range and High Frame-Rate Machine Vision Imaging Applications", *IEEE Sensors Journal*, Vol. 15, No. 7, pp. 4121-4129, 2015

[3] Z. Gao, S. Yao, C. Yang and J. Xu, "A Dynamic Range Extension Technique for CMOS Image Sensor With In-Pixel Dual Exposre Synthesis", *IEEE Sensors Journal*, Vol. 15, No. 6, pp. 3265-3273, 2015

[4] M. I. Abedin, A. Islam and Q. D. Hossain, "A self-adjusting Lin-Log active pixel for wide dynamic range CMOS image sensor", *2015 IEEE International Conference on Telecommunications and Photonics*, pp. 1-4, 2015

[5] D. Park, J.R. Hee, and Y. Joo, "Wide Dynamic Range CMOS Image Sensor Using Self-reset Technique", *IEEE Electron Device Letters*, Vol. 28, No. 10, pp. 890-892, 2007

[6] G. C. Harendt, T. Engelhardt, C. Scherjon, K. Warkentin, H. Richter, and J. N. Burghartz, "High dynamic range CMOS imager technologies for biomedical applications", *IEEE Journal of Solid-State Circuits*, Vol. 44, No. 1, pp. 281-288, 2009

[7] S. E. Kemeny, R. Panicacci, B. Pain, L. Matthies and E. R. Fossum, "Multiresolution Image Sensor", *IEEE Trans on Circuits and System for Video Technology*, Vol. 7, No. 4, 1997

[8] M. W. Seo, T. Sawamoto, T. Akahori, T. Iida, T. Takasawa, K. Yasutomi., and S. Kawahito, "A Low Noise Wide Dynamic Range CMOS Image Sensor With Low-Noise Transistors and 17b Column-Parallel ADCs", *IEEE Sensors Journal*, Vol. 13, No. 8, pp.2922-2929, 2013