Optimization of pixel structure for reducing knee point variation in the logarithmic response of linear-logarithmic CMOS image sensor

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Abstract We propose a linear-logarithmic CMOS image sensor with a modifiable dynamic range by adjusting the reference voltages. To implement these characteristics, a photogate and a MOS cascode are integrated with the pixel structure in conjunction with the photodiode. The new linear-logarithmic pixel is based on a conventional 3-transistor active pixel sensor structure. In addition, we propose the optimized pixel with reduced knee point variation in the logarithmic response. The proposed pixel has been designed and fabricated using a 0.35-μm 2-poly 4-metal standard CMOS process.

Keywords: CMOS image sensor, linear-logarithmic response, wide dynamic range

1. Introduction

Recently, the CMOS active pixel sensor (APS) has been used in a wide variety of applications, including digital camera and mobile phones. The APS usually consists of a 3-transistor (3-Tr) APS or a 4-transistor (4-Tr) APS. The pinned photodiode based 4-Tr APS structure has been favorably used in the APS due to the performance advantages of low dark current and high sensitivity compared to the 3-T pixel structure [1]. However, the pinned photodiode based 4-Tr APS has some disadvantages, such as a small fill factor emerging from the use of additional transistors, a low dynamic range (DR) associated with the small well capacity, and high cost due to the required modification in the typical CMOS process [2].

Various approaches have been proposed to attain high-sensitivity and wide dynamic range [3][4]. In order to extend the dynamic range of the pixel, addition of devices or circuits is inevitable. According to an increase of device in the pixel, many problems are beginning to emerge. It is show a decrease the photodetector's area in the pixel and a decline of the fill factor. If the devices which constitute the pixel occur non-uniformity, the pixel shows a variation in characteristics.

We had been proposed a linear-logarithmic CMOS image sensor with a modifiable dynamic range by adjusting the reference voltages [5][6]. In this paper, we propose the optimized linear-logarithmic pixel with reduced knee point variation in the logarithmic response. The proposed pixel has been designed and fabricated using a 0.35-μm 2-poly 4-metal standard CMOS process.

2. Pixel Structure

The proposed linear-logarithmic pixel schematic diagram is illustrated in Fig. 1. This is equivalent-circuit diagram of the new pixel structure for the desired second linear operation and controllability of the proposed structure, a positive bias voltage (V_{lin}) is applied at the photogate. The new pixel structure is designed to be similar to a conventional 3-Tr APS structure. The overall photosensing part of the new structure is composed of both a photogate region and a photodiode region, as shown in Fig. 1. The logarithmic response is guaranteed by a MOS cascode (M4 and M5), with the gate connected to the drain.

Although the dynamic range of the pixel has been improved, each pixel's output curves were not uniformed. As the number of device increased in the pixel, it shows that output of pixels have different values at the same light intensity. A mismatch of the device play an important role in output tolerance. Hence, we propose optimized pixel structure for the minimize tolerance. The optimization has been ascertained through the change of gate. The MOS cascode of the optimized pixel has gate length and width.

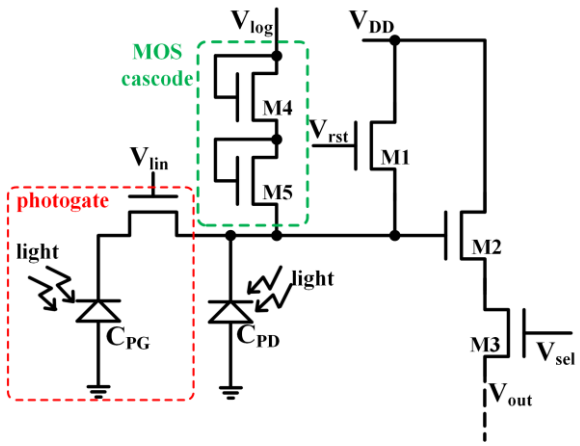
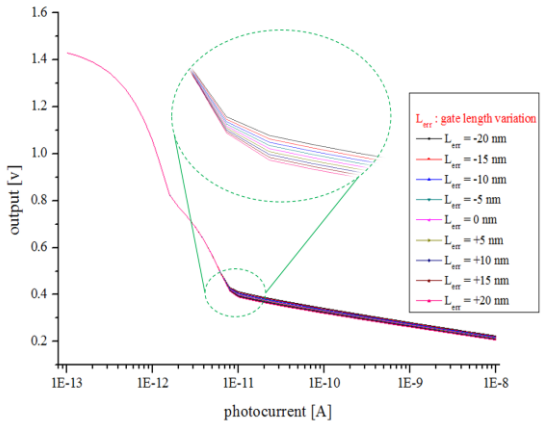


Fig. 1. Schematic diagram of the proposed pixel.

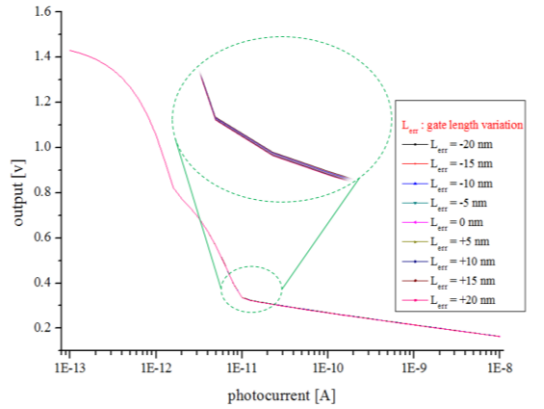
3. Measurements

Figure 2 shows simulation results which variances of the conventional linear-logarithmic pixel's output curve (a) and optimized linear-logarithmic pixel's output curve (b) as a function of

the gate length variation (L_{err}). The MOS cascode of the optimized pixel has gate length and width as double as that of the conventional pixel. Unlike conventional pixel, the optimized pixel has less tolerance as shown Fig. 2.



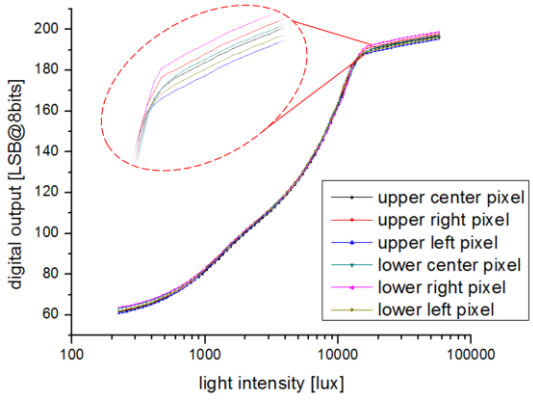
(a)



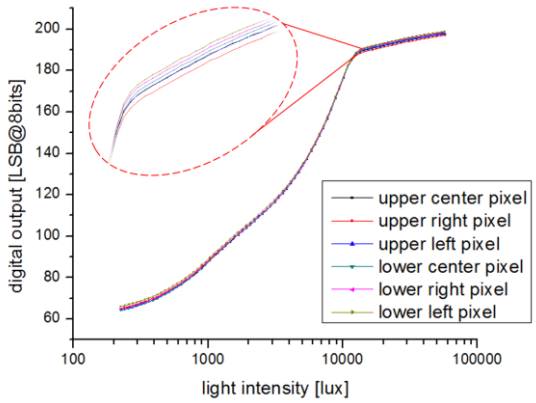
(b)

Fig. 2. Variances of the conventional linear-logarithmic pixel's output curve (a) and optimized linear-logarithmic pixel's output curve (b) as a function of the gate length variation (L_{err}).

Figure 3 shows measurement results which variances of the conventional linear-logarithmic pixel's output curve (a) and optimized linear-logarithmic pixel's output curve (b) as a function of sample pixel in the image sensor. The results are similar to the simulation results, as shown Fig. 2. The optimized pixel shows less output tolerance in logarithmic response because it has a large MOS cascode.



(a)



(b)

Fig. 3. Variances of the conventional linear-logarithmic pixel's output curve (a) and optimized linear-logarithmic pixel's output curve (b) as a function of the sample pixel.

4. Conclusions

We proposed a linear-logarithmic APS with a wide dynamic range and a technique of reduction knee point variation. The proposed APS and optimized APS have been designed and fabricated using a 0.35-μm 2-poly 4-metal standard CMOS process. We achieve a reduction of knee point variation which generated by the non-uniformity of device at the logarithmic response.

Acknowledgments

This work was supported by Samsung Electronics Co., Ltd, BK21 Plus project funded by the Ministry of Education, Korea (21A20131600011), and the Integrated Circuit Design Education Center (IDEC) in Korea.

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