Design and fabrication of a low power terahertz imager based on 180 nm CMOS process technology

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Abstract A low power terahertz imaging using CMOS detector and analog-to-digital conversion (ADC) is proposed. For terahertz detection, a CMOS cascade amplifier, biased near the threshold voltage of a MOSFET, is utilized. A 16 x 16 pixel imaging array with the 256 column ADCs is designed using 180 nm CMOS process technology. Measured result for the pixel circuit is presented. The imaging pixel consists of a microstrip patch antenna, an impedance-matching circuit, and a direct detector. It achieves a responsivity of 51.9 kV/W at 0.915 THz and noise equivalent power (NEP) of 358 pW/Hz$^{1/2}$ at modulation frequency of 31 Hz. NEP is estimated to be reduced to 42 pW/Hz$^{1/2}$ at 100 kHz. The detector only draws about 3 µA from a power supply (V_{dd}) of 1.5 V.

Keywords: terahertz, thz, imager, CMOS, detector, imaging, responsivity, NEP, on-chip patch antenna, microstrip antenna, direct detection, envelope detection, imaging array, low power

1. Introduction

The terahertz-frequency region (100 GHz – 10 THz), namely, between millimeter-waves and far-infrared light waves, has attracted much attention owing to its wide range of applications (such as wireless communications and sensors). Terahertz waves, which pass through a wide variety of substances, such as plastics, fabrics, and paper, can reveal hidden contents that cannot be seen by visible light [1][2][3]. In addition, so-called fingerprint spectra in the terahertz frequencies can identify hazardous materials.

However, the lack of low-cost and small-size microelectronics that generate sufficient power and detect a faint signal (often called the "THz gap") is one of the major obstacles preventing terahertz applications from coming into wide use in our daily live [4]. In the microelectronics community, terahertz detection outperforms terahertz generation. Detection methods are generally divided into two kinds, namely, coherent (heterodyne) detection and incoherent (direct) detection. Although heterodyne detection achieves higher sensitivity than direct detection, it requires a local oscillator and mixer that are difficult to construct with today's technology. Direct detection is favorable to imaging applications, where the power consumption per pixel needs to be small to achieve a large-size array. For those reasons, direct detection has been used. Terahertz direct detectors have primarily relied on specialized fabrication technologies such as Schottky diodes [5], bolometers [6], and high-electron-mobility transistors [7]. Many of these technologies require additional process steps to make them compatible with CMOS technologies [8]. Silicon-CMOS process technologies are becoming a cost-efficient alternative. The main advantage of silicon technologies is that they allow low-cost and large-scale integration of circuits by using readout electronics and on-chip signal processors [9]. Furthermore, the high-frequency capabilities of silicon technologies have steadily improved in accordance with the guiding principle of scaling, which enables high integration level and low power consumption at higher frequencies [10]. In this paper, we mainly address our pixel-circuit design and its measurement.

2. Design of terahertz imager

For terahertz-wave detection, non-linearity of a nMOSFET is utilized. The nMOSFET is biased near the threshold voltage. The circuit shown in Fig.1 was used as an envelope detector. It consists of a cascode-amplifier circuit and a subthreshold-biased operational amplifier (subVth-OP amp). The former consists of a common-source nMOSFET M3 as the input stage driven by terahertz signal V_{IN} with common-gate MOSFET M2. And pMOSFET M1 is the load. The cascode-amplifier circuit operates as an envelope detector. The subVth-OP amp operates as a feedback circuit, which determines the load resistance of M1 [11]. Output voltage of the detector is fixed to common-mode voltage V_{CM} at the DC level. Since the subVth-OP amp operates very slowly with a large time constant, the feedback operation is established only at DC and very low frequencies. The feedback circuit operates as a high-pass filter in the detector. Therefore, the envelope detector with the feedback subVth-OP amp produces no DC offset voltage in its output.

A chip layout of the designed terahertz imager is shown in Fig. 2. It consists of a 16 x 16 pixel imaging array and 256 column ADCs. The size is 5 mm x 5 mm. The imaging pixel was composed of a microstrip patch antenna, matching circuit, and detector.

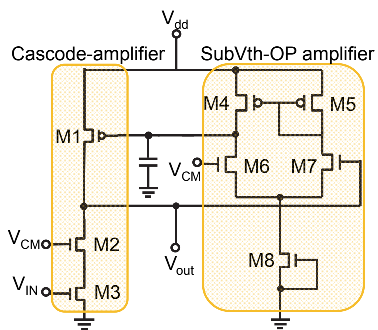

Fig.1 .Schematic of detector circuit

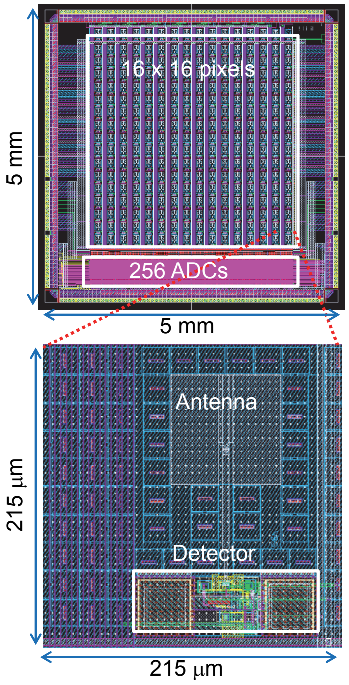

Fig. 2. Chip layout of terahertz imager

3. Measurement results for the pixel circuit

Before evaluating the whole imager, the fabricated pixel TEG was measured. For responsivity measurements, an injection-seeded terahertz-wave parametric generator (is-TPG) was used as a frequency-tunable terahertz-wave source [12]. The responsivity of the pixel was calculated from detected output voltage divided by available power to the antenna. The peak responsivity at 0.915 THz is 51.9 kV/W.

Measured output noise and gain for a detector with the same circuit configuration as the pixel in the terahertz imaging array (except for the antenna and matching circuit) is shown in Fig. 3. At modulation frequency of 31 Hz, output noise level is 18.6 µV/Hz$^{1/2}$, and measured NEP is 358 pW/Hz$^{1/2}$. NEP can be decreased by increasing sampling rate. Since the measured imaging array excludes an output buffer, the operation bandwidth of the detector with the extremely small current is degraded by the parasitic capacitances in the measurement equipment. If the parasitic capacitances of the measurement equipment are taken into account, simulated gain well matches measured gain (simulation A in Fig. 3). The operation bandwidth in the pixel circuit can be increased (corresponding to simulation B in Fig. 3). By increasing sampling rate, NEP of 42 pW/Hz$^{1/2}$ is expected to be obtained at 100 kHz.

The detector only draws about 3 µA from a power supply (V_{dd}) of 1.5 V.

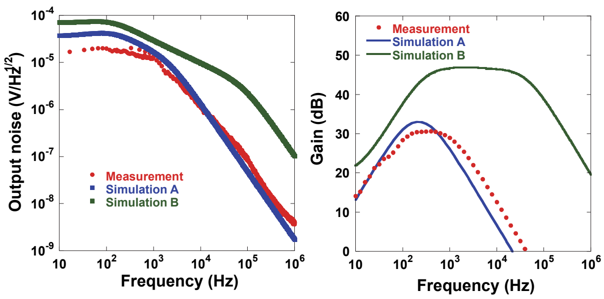

Fig. 3. Measured output noise and gain

Simulation A: with taking into account the parasitic capacitances in the measurement equipment (BNC cable and FRA). Simulation B: operation in the pixel circuit.

4. Conclusion

A terahertz imager based on 180 nm CMOS process technology was designed and fabricated. The detector achieves a responsivity of 51.9 kV/W at 0.915 THz and a NEP of 358 pW/Hz$^{1/2}$ at modulation frequency of 31 Hz. The detector's large NEP is mainly due to low modulation frequency. And it can achieve NEP of 42 pW/Hz$^{1/2}$ by increasing its modulation frequency to 100 kHz. The detector only draws about 3 µA from a power supply (V_{dd}) of 1.5 V. That means the detector has extremely low power consumption and is thus well suited for constructing a large-size array of imaging detectors. These results suggest that cost-efficient terahertz imaging is possible. Measured results for the fabricated imager will be reported in the near future.

Acknowledgements

This work was supported by the Ministry of Internal Affairs and Communications of Japan / Strategic Information and Communications R&D Promotion Programme (MIC/SCOPE) #151301001 and the VLSI Design and Education Center (VDEC), University of Tokyo in collaboration with Cadence Design System, Inc. and Keysight Technologies Japan, Ltd.

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