[Poster Presentation] An 8-tap CMOS Lock-In Pixel CMOS Image Sensor for Real-Time Biomedical Imaging Application

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Abstract In this paper, we has proposed a new pixel design, which detects and transfers photo-induced charges to eight storage diodes (SD), and its effectiveness is demonstrated by a device simulation. The proposed pixel makes possible to measure the highly time-resolved imaging with a high signal to noise ratio and to observe various imaging of cells having different fluorescence lifetime in real time.

Keywords: CMOS image sensor, 8-tap CMOS lock in pixel, real-time biomedical imaging, time-resolved imaging, lateral electric field charge modulator, charge-transfer assist gate

1. Introduction

Recently, CMOS time-resolved imaging devices are expected to be used for scientific and medical applications. A fluorescence lifetime imaging microscopy (FLIM), which is a powerful analysis tool in fundamental physics as well as in the life sciences, is a representative application of the time-resolved imaging devices.

For better time-resolution in the lock-in pixel design, the number of time-windows and multiple outputs are required to be as many as possible. High-performance multi-tap CMOS image sensors have been designed in previous studies, e.g., 2-tap CMOS image sensor and 4-tap CMOS image sensor [1], [2]. We have designed an 8-tap CMOS lock-in pixel CMOS image sensor for realizing the highly time-resolved imaging with a high signal to noise ratio (SNR) in real time. In particular, the proposed pixel allows to observe various imaging of cells having different fluorescence lifetime components.

2. Lateral electric field charge modulator (LEFM)

Fig.1 shows the structure of a two-tap LEFM lock-in pixel and the potential diagrams when the gate voltages (TG1 and TG2) are changed. This structure has two gates (TG1, TG2) and these gates make it possible to transfer signal electrons generated in Photodiode (PD), from the PD to floating diffusion (FD) node by controlling lateral electric field. As it can be seen from Fig.1, the signal electrons are transferred to the right-hand side of the PD when a low negative voltage (-2V) and a high positive voltage (1V) are applied to TG1 and TG2, respectively. When the opposite supply voltages for TG1 and TG2 are applied, the signal charges are transferred to the left-hand side of the PD. The transfer method using the LEFM in good for highly time-resolved imaging because a potential barrier which causes charge transfer delay is not generated on the charge transfer channel [3].

3. 8-tap CMOS lock-in pixel structure

Fig.2 shows an 8-tap CMOS lock-in pixel structure. The proposed pixel contains several unique structures for high-speed charge transfer and increasing full well capacity.

3-1. W-shaped pixel

The pixel consists of a pinned photodiode (PPD), eight storage diodes (SDs), eight sets of LEFMs (TG1 to TG8), eight FD nodes which are connected to each individual in-pixel source follower (SF) amplifier.

The proposed pixel transfers the signal charges from the PD to eight SDs by using TG1 to TG8. To attain the large fill factor (FF) for improving their sensitivity, special design technique is required, because the channel potential at the center of the PD is hard to be controlled by the lateral electric fields. Thus, we propose a W-shaped pixel, whose naming comes from the cross-sectional potential shaped like the letter of “W” as it can be seen from Fig.3. Fig.3 shows the simulation results for the potential diagram along with X-X' when charges generated in the PD are transferred to the SD7. This is formed by removing the small n-type doping layer (PUP: pull-up point) at the center in the PD, and the signal charges flow along with the formed potential valley around the PUP.

In this pixel, two different types of LEFM gate voltages, which are the intermediate voltage levels (V_{M1} and V_{M2}) between V_H and V_L (see Fig.2) for higher-speed charge transfer.

Fig.4 shows plots of the equipotential lines and carrier transportation. A red point denotes the initial position of an electron generated by a photon and a black-dotted line indicates the movement trace of an electron. We confirmed that this pixel can transfer charges to the targeted SD by this simulation result.

3-2. Charge transfer assisting gate

Fig.5 shows the structure of a charge transfer assisting gate (CA) and potential diagrams by varying the gate voltages (V_{TG} and V_{CA}) in accumulation mode and transfer mode. The CA structure is composed of a set of two gates which are placed on both sides of the SD. The CA makes possible to increase a full well capacity of the SD and help to transfer the charges to the FD node from the SD.

As it can be seen from Fig.5(b), when the signal electrons are accumulated in the SD, a high positive voltage (2.3V) are applied to the CA for increasing full well capacity. As shown in Fig.4(c), when the signal electrons accumulated in the SD are transferred to the FD, a low negative voltage (-1.0V) are applied to the CA for facilitating the transfer process between the SD and FD.

4. Conclusion

In this report, we propose an 8-tap CMOS lock-in pixel with the LEFM and demonstrate the effectiveness by device simulation. We confirmed that 8-tap CMOS lock-in pixel can transfer charges to the targeted SD and the CA structure makes possible to increase a full well capacity of the SD by this simulation result.

Acknowledgments

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References

[1] Min-Woong Seo et al, "A 10ps Time-Resolution CMOS Image Sensor With Two-Tap True-CDS Lock-In Pixels for Fluorescence Lifetime Imaging" IEEE J. Solid-State Circuits, vol.51, no. 1, pp. 141-154, Jan. 2016.

[2] Taichi Kasugai et al, "A Time-of-Flight CMOS Range Image Sensor Using 4-Tap Output Pixels with Lateral-Electric-Field Control" IS&T Internal Symposium on Electronic Imaging, Image Sensor and Imaging Systems, pp. 048.1-048.6, Feb, 2016.

[3] S. Kawahito et al, "CMOS lock-in pixel image sensors with lateral electric field control for time-resolved imaging" in Proc.Int.Image Sensor Workshop (IISW), Snowbird, UT, USA, pp.361-364, Jun.2013.

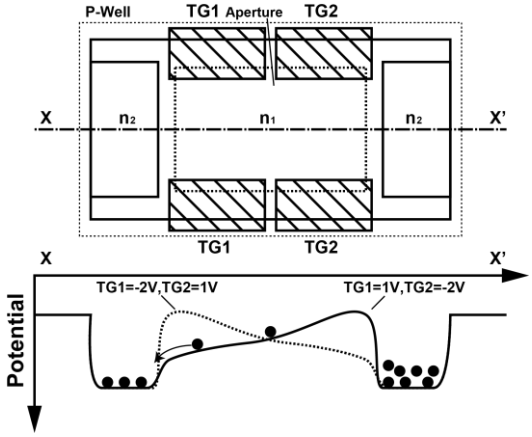


Fig1: The structure of a two-tap LEFM lock-in pixel and the potential diagrams

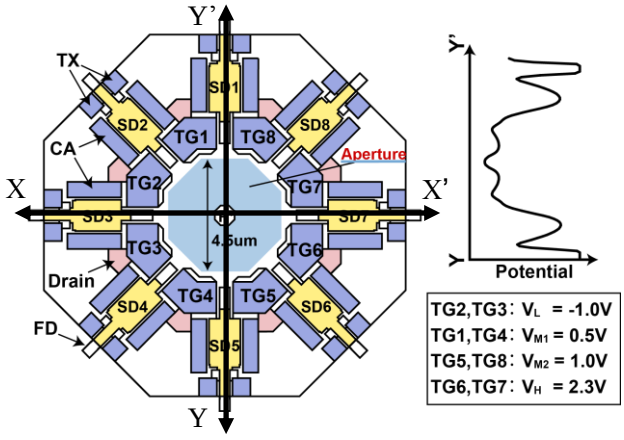


Fig2: 8-tap CMOS lock-in pixel structure

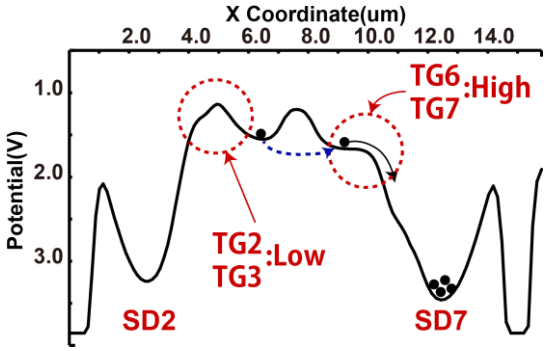


Fig3: The simulation results for the potential diagram from SD3 to SD7

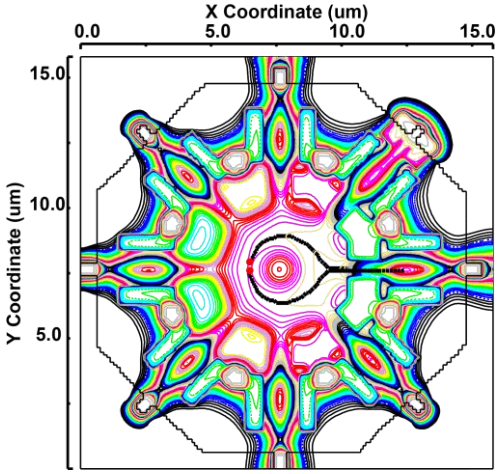
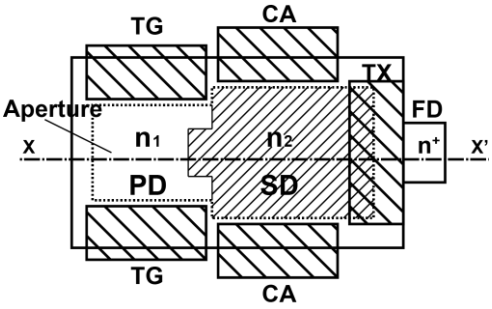
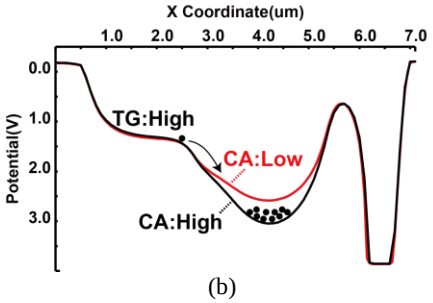


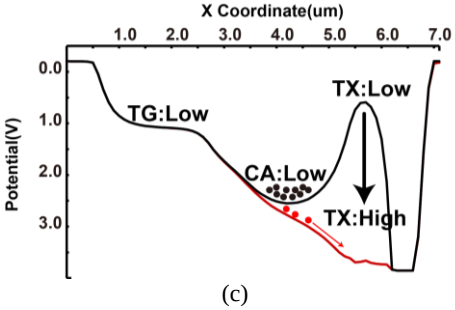
Fig4: Plots of the equipotential lines and carrier transportation



(a)



(b)



(c)

Fig5: The CA structure. (a) Layout. (b) Accumulation mode (c) Charge transfer mode