A Lateral Electric Field Charge Modulator with Bipolar-gates for High Time-Resolved Imaging

Yuki Morikawa† Keita Yasutomi† Shoma Imanishi† Taishi Takasawa†
Keiichiro Kagawa† Nobukazu Teranishi† Shoji Kawahito†
†Research Institute of Electronics, Shizuoka University,
3-5-1 Johoku, Naka-ku, Hamamatsu, Shizuoka, 432-8011, Japan
E-mail: †{ymori, kyasu, kawahito}@idl.rie.shizuoka.ac.jp

Abstract This paper reports high time-resolved imaging technique using a lateral electric field charge modulator with bipolar-gates. The proposed pixel structure achieved high time-resolved signal detection by using negative bias effect by work function difference between the p-type gate and p-substrate. The test chip fabricated in 0.11 um CIS technology demonstrates the hole attraction effect, and the modulation contrast is measured to be 97%.
Keywords: CIS, Time-resolved IS, TOF, Lateral-Electric-Field charge Modulator, negative gate biasless

1. Introduction

Time-resolved lock-in pixel image sensors have wide range of applications such as time-of-flight (TOF) range imaging [1-2] and biological imaging with fluorescence lifetime imaging microscopy (FLIM) [3-4]. Time-resolved imaging requires an imager with very high-speed charge modulation, high modulation contrast, loss-less accumulation because it is necessary to detect phenomena which occur in a very short period of time. To do this, a lateral-electric-field charge modulator (LEFM) have been proposed [5]. Since the LEFM pixel does not have any transfer gates in a signal path, high-speed charge modulation can be achieved.

Conventional LEFMs, however, requires a negative gate bias to enhance a potential change in the channel. A negative power supply with low impedance is necessary in the camera system. In addition, the requirement of negative bias becomes a problem to introduce an in-pixel buffer, which is effective to keep high-speed charge modulation for two-dimensional pixel array [6]. This is because it is necessary to add an isolation layer (Deep N-well) with a substrate to implement the in-pixel buffer, and this leads to significant reduction of fill factor.

This paper presents a LEFM with bipolar-gates. The proposed pixel structure uses negative bias effect by work function difference between the p-type gate and p-substrate. By using this structure, the negative power supply is unnecessary, and the isolation layer also can be removed to implement the in-pixel buffer. Thus, it is possible to obtain a high-speed charge modulation while maintaining a high fill factor.

2. Pixel structure

Fig. 1 shows the conventional two-tap LEFM, in which two sets of gates (G1 and G2) creating a lateral electric field are used. The gates are not used for transferring charge through the gate, but for controlling electric field of X-X' direction by changing the hole concentration of the pinned photo diode surface. To do this, a positive voltage (HIGH=2.0V) and negative voltage (LOW=-1.0V) are used for the operation. The direction of electron flow in a pinned photodiode is controlled by the gates, and time-resolved signal detection and accumulation are carried out in the two floating diffusions (FD1 and FD2). During signal readout, GD is ON and other gates are OFF for preventing the influence of background light.

Fig. 2 shows the structure and potential of the three-tap LEFM with bipolar-gates. The proposed pixel structure employs p-type gates as well as n-type gates unlike the conventional structure in which the only n-type gates is used. We call this gate structure the bipolar-gates. Since the bipolar-gates structure helps to attract holes at zero bias by work function difference between the p-type gate and p-substrate. The negative gate bias is not required in the modulation pulses. Only a positive voltage (HIGH=2.5V) is used. A low voltage is connected a ground voltage (0V). The bipolar-gates structure has a larger potential modulation than the n-type gates structure by work function difference between the p-type gate and p-substrate. In multiple-tap (three or more taps) CMOS lock-in pixel, distance or lifetime is measured with background light cancelling capability in one frame.

To investigate negative bias effect of p-type gate, simple LEFM structures with n / p-type gates are simulated by device simulator, as shown in Fig. 3(a). The 3D device simulation was performed by SPECTRA. Fig. 3(b) shows simulated channel potential as a function of the gate voltage for various widths of the p-type gate and n-type gate. From this result, as the width of p-type gate is wider, the onset of “pinning” at the channel shifts to higher gate voltage. The channel potential of all n-type gate is pinned at -1.0V, while that of all p-type gate is pinned at 0V. In other words, all p-type LEFM with 0V bias is equivalent to all n-type gate with -1.0V bias.

3. Measurement result

To prove the concept of the proposed three-tap bipolar-gates structure, a test chip is fabricated in a 0.11um CIS technology. Fig. 4 shows the modulation method for three-tap LEFM. TOF calculation is performed by outputs of FD1 and FD2. By subtracting the output of FD3 from FD1 and FD2, the background light is canceled. In the measurement setup, a 448nm laser with a pulse width of 72 ps is used for the light source. The emission trigger of the laser is given by the sensor board via a digital delay generator (DDG) which can accurately control the delay time of laser trigger. The change of trigger delay is equivalent to the change in the time-of-flight. The high level for gate voltage of G1, G2, G3 and GD is set to 2.5V, and the low level is set to 0V. Fig. 5 shows normalized pixel outputs: N1, N2, N3, and the differential value of N2 as a function of the trigger delay. The differential value of N2 corresponds to the photocurrent. As the delay of laser trigger increases, the output of N2 increases due to the following reason. When the delay equals zero, since the received light is earlier than the rising edge of G2 pulse, all the photocurrent flow into the FD1. As the delay increases, the falling edge of the photocurrent is first included inside G2 open time or accumulated in the FD2. The rising edge is then accumulated.

The rising and falling time of photocurrent are measured to be 200 ps and 400 ps, respectively. The modulation contrast is also measured to be 97%.

4. Conclusion

This paper presented a new LEFM structure using bipolar-gates. The proposed structure uses negative bias effect by work function difference between the p-type gate and p-substrate. The test chip fabricated in 0.11 um CIS technology demonstrates the high-speed photocurrent response, and the high time-resolved imaging. This structure is expected to improve the time resolution in fluorescence lifetime imaging and TOF range imaging.

5. Acknowledgements

This study was partly supported by A JSPS KAKENHI Grand Number JP25220905, JP15H05524, JP15K13973 and the Center of Innovation Program. The chip design was also supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Mentor Graphics, Inc. The authors appreciate Dongbu HiTek for CIS fabrication.

References

[1] S-M. Han, et al., "A 413×240-pixel sub-centimeter resolution Time-of-Flight CMOS image sensor with in-pixel background canceling using lateral-electric-field charge modulators," ISSCC Dig. Tech. Papers, pp. 130-131, Feb. 2014.

[2] T. Kasugai, et al., "A time-of-fight CMOS range image sensor using 4-tap output pixels with lateral-electric-field control," Electronic Imaging 2016, Feb. 2016.

[3] Min-Woong Seo, et al. "A 10ps Time-Resolution CMOS Image Sensor With Two-Tap Ture-CDS Lock-In Pixels for Fluorescence Lifetime Imaging" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 51,NO.1

[4] Z. Li, S. Kawahito, K. Yasutomi, K. Kagawa, J. Ukon, M. Hashimoto,and H. Niioka, "A time-resolved CMOS image sensor with draining-only modulation pixels for fluorescence lifetime imaging," IEEE Transactions on Electron Devices, Vol.59, No.10, pp.2715-2722, Oct. 2012

[5] S. Kawahito et al., "CMOS lock-in pixel image sensors with lateral electric field control for time-resolved imaging," in Proc. Int. Image Sensor Workshop (IISW), pp. 361–364, Snowbird, UT, USA, Jun. 2013.

[6] K.Yasutomi, et al., "A 0.3mm-Resolution Time-of-Flight CMOS Range Imager with Column-Gating Clock-Skew Calibration," Dig. Tech. Papers, IEEE Int. Solid-State Circuits Conf.(ISSCC), pp.132-133, Feb. 2014.

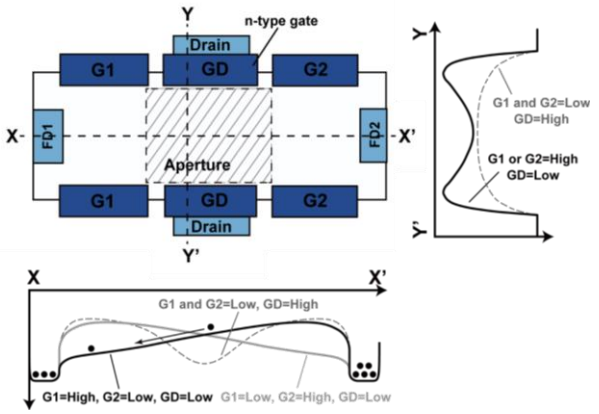


Figure 1. The conventional two-tap LEFM with Drain

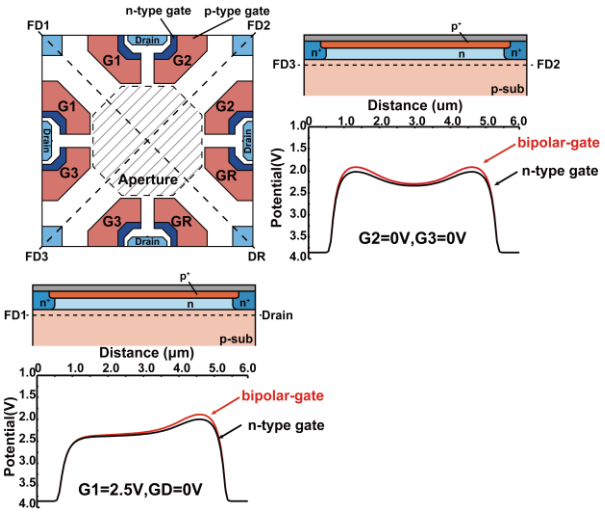
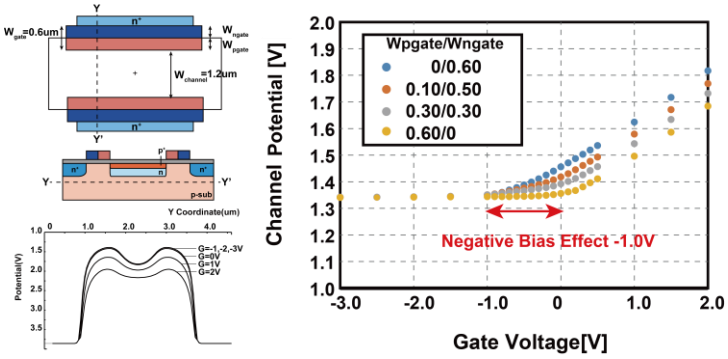


Figure 2. The three-tap LEFM with bipolar-gates



(a) (b)

Fig 3. Simulation structure and result

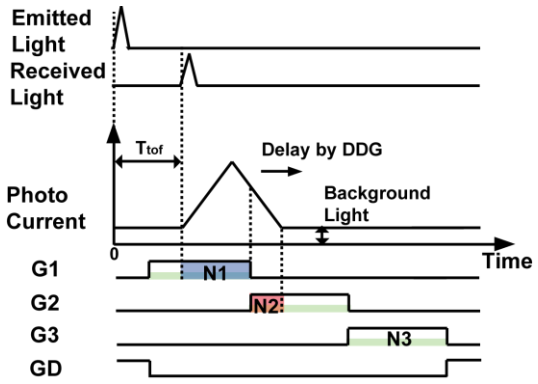


Figure 4. Modulation method for the three-tap LEFM

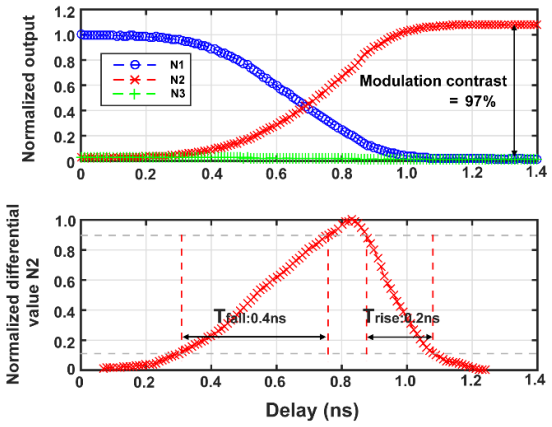


Figure 5. Modulation charastaristic