A Dedicated Image Processing Engine Stacked with CMOS Image Array at 40nm CMOS Imager Technologies

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Abstract Current camera systems present a huge image signal processing (ISP) programmable limitation, since the ISP algorithm is mainly hard-coded via Application Processor. We'll present the prototype development result of a Re-Configurable Instruction Cell Array (RICA), a real time, low power reprogrammable ISP engine stacked with 8MP detector array fabricated in 40nm BSI CMOS imager technology. We believe this RICA stacked image sensor technology presents an efficient programmability solution to support adjacent IOT markets, and next generation computational camera technologies.

Key Words Re-Configurable Instruction Cell Array (RICA), Stacked BSI Image Sensor, Computational Photography

1. Introduction

Traditional camera system is generally a dedicated and standalone system, which consists of discrete optics, image sensor, and processing engine. Although it's a mature solution, however, this represents an expensive system solution, many custom parts, and complex image quality tuning ISP. As the paradigm shift toward mobile compoutational photography, it's essential to migrate from the discrete camera systems into integrated imaging and digital optics, so as to compensate computationally of technology limitations. Therefore, the concept of computational camera consists of integrated optics, integrated sensor, processing, multifunction system, which offers a fully integrated system solution with complex image tuning replaced by software programmability.

It has become apparent that the Next-Gen of camera systems will be computational, and closed coupled to optics & processing. Even today the variety of available image sensor technologies make programmable architectures the preferred solution. A Re-Configurable Instruction Cell Array (RICA)[1] has been developed with architecture aiming for high speed streaming application. This processing architecture is suitable as programmable imaging & video processor. It features reconfigurable core for multiple applications, which offers the great benefits of configurable like FPGA, programmability like DSP, and speedy like hardwired solutions. With the availability of stacked image sensor technologies, it presents an opportunity to insert RICA into the stacked sensor implementation.

2. Device Formation

We have designed & fabricated a RICA ASIC wafer stacked with a pixel arrays wafer of 8MP, 1.1um pixel BSI CMOS image sensor with low noise readout as the test vehicle, as illustrated in Fig-1. This device take advantage of the matured hybrid bond stacked technologies[2] at 40nm CIS BSI processed at TSMC. The pixel architecture adopts a 2x2-shared in order to gain pixel cell utilization as photo-detector. Design of the low readout noise imager adopts readout architecture comprises a column amplifier, a comparator, and a 10 to 12-bit programmable column parallel Single-Slope ADC along with a global 12-bit current DAC, which is programmable to generate various slope of ramp signals with implemented timing schemes to suppress readout noise. The circuit blocks partition strategy is consists of detector array and vertical scanner in array wafer stacked bonded with ASIC wafer, which includes RICA ISP, and imager sensor readout peripheral circuitry.

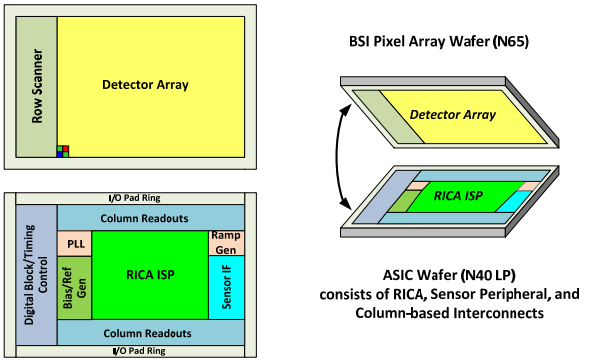

Figure 1. Stacked RICA ASIC wafer with Detector Array wafer of circuit partition.

The Re-Configurable Instruction Cell Array is a coarse heterogeneous FPGA, which is C-programmable with multiple configurations that are conditionally located in real time. The instruction cells are 16-bit with ALU, MUL, SBUF, SINK, and SOURCE as illustrated in Fig-2. It also consists of wide program memory with configuration, and operates variable clock rates at each step. The parallelism of data and minimal clock are C-programmable, making RICA running at the lowest clock speed for a particular implementation. This solution presents unsurpassed advantage of running image processing engine at the pixel clock, which save substantial power as oppose to running ISP chains in the Application Processor

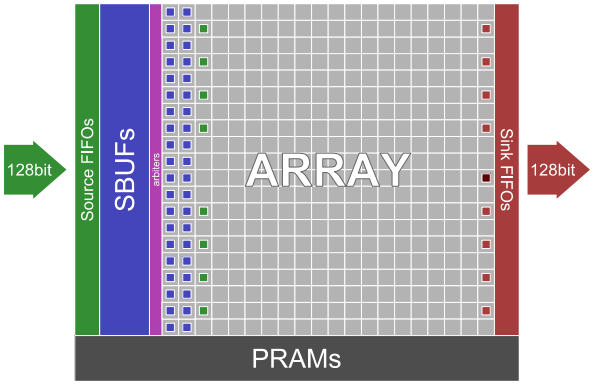

Figure 2. Graphic representation of Silicon layout for RICA core.

3. Device Characteristics

The device performance of the imager array features reasonable low dark current & hot pixel distribution, and linear

full well capacity of 4800-e, with sense node conversion gain of 120uV/e, and sensitivity of 4200 e-lux-sec @530 nm. The read noise is measured at 8X analog gain, and input referred of 2.2-e_rms has been achieved. The photo-response characteristics, such as non-uniformity, non-linearity & blooming ratio, are pretty much intact as compared to the leading edge CMOS imager solutions. Furthermore, the stacked image sensor performance is not degraded from its non-stacked imager counterpart, and in some cases, outperforms the BSI baseline. The summarized device key performance indices are listed in Table-1.

Performance Indices		1.1um
Dark Current @ 60 ºC	e/sec	5
Hot Pixel > 140-e/s	ppm	500
Read Noise	e	2.2
RTS @99.9%	e	7.2
FWC_linear	e	4800
Sensitivity @530nm	e/lux-s	4200
PRNU	%	0.7
PRNL	%	< 5
Blooming Ratio	%	<3
Image Lag	e	< 1
QE_max@530nm	%	73

Table 1. Device key performance indices measure

The spectral response curves of the 1.1um pixel device is illustrated in Fig. 3. Color Correction Matrix was extracted from the QE curves to achieve white balance & combat pixel cross-talk and color separation. We can also examine our de-mosaic algorithm robustness via RICA on mitigating the intrinsic cross-talk of small pixel, and maintain the trade-off balance between SNR and color error.

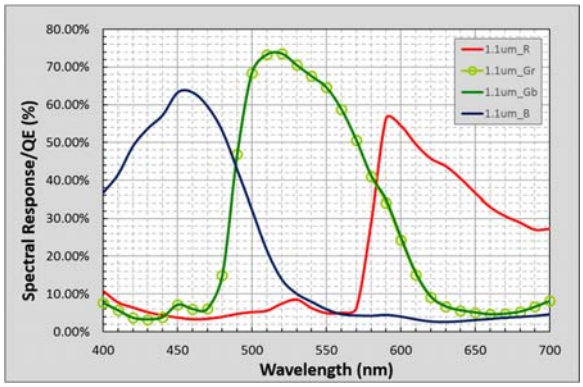

Figure 3. QE plot of detector array

4. Image Processing

The Universal De-mosaic algorithm [3] was applied to process the raw image data captured with the stacked imager, which illustrated superior image fidelity with PSNR of 40.7, 41.5, & 39 dB in Red/Green/Blue color channels respectively, which were averaged across 6-patch of Macbeth Color Chart. The final processed image is shown in Fig-4.

Figure 4. Image after universal de-mosaic processing

In addition to the visible imaging application, other use cases in the NIR sensing, including structured light depth sensing, 3D scanning, object recognition, & bio-sensing etc., the RICA stacked imager solution represents a flexible image processing engine and enable fast prototype of camera systems in the emergent adjacent markets.

5. Conclusion

We have designed and prototyped a dedicated image signal processing engine stacked with an 8MP image array in 4onm CMOS BSI image sensor & ASIC technologies. The demonstrated stacked Silicon solution will enable flexible and efficient programmable ISP chains to enable emergent digital imaging applications, and future computational photography.

6. References

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